**STM32L031x4 STM32L031x6**

Access line ultra-low-power 32-bit MCU Arm~~®~~-based Cortex®-M0+, up to 32KB Flash, 8KB SRAM, 1KB EEPROM, ADC **Datasheet** - **production data**

**Features**

• Ultra-low-power platform

– 1.65 V to 3.6 V power supply

– -40 to 125 °C temperature range

– 0.23 µA Standby mode (2 wakeup pins) – 0.35 µA Stop mode (16 wakeup lines)

– 0.6 µA Stop mode + RTC + 8 KB RAM retention – Down to 76 µA/MHz in Run mode

– 5 µs wakeup time (from Flash memory) – 41 µA 12-bit ADC conversion at 10 ksps • Core: Arm® 32-bit Cortex®-M0+

– From 32 kHz up to 32 MHz max.

– 0.95 DMIPS/MHz

• Reset and supply management

– Ultra-safe, low-power BOR (brownout reset) with 5 selectable thresholds

– Ultralow power POR/PDR

– Programmable voltage detector (PVD) • Clock sources

– 1 to 25 MHz crystal oscillator

– 32 kHz oscillator for RTC with calibration – High speed internal 16 MHz factory-trimmed RC (+/- 1%)

– Internal low-power 37 kHz RC

– Internal multispeed low-power 65 kHz to 4.2 MHz RC

| WLCSP25  TSSOP20  LQFP32/48  UFQFPN28 4x4 mm  2.097x2.493 mm  169 mils  7x7 mm  UFQFPN32 5x5 mm  UFQFPN48 7x7 mm |
| --- |

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• Rich Analog peripherals

– 12-bit ADC 1.14 Msps up to 10 channels (down to 1.65 V)

– 2x ultra-low-power comparators (window mode and wake up capability, down to 1.65 V)

• 7-channel DMA controller, supporting ADC, SPI, I2C, USART, Timers

• 5x peripherals communication interface • 1x USART (ISO 7816, IrDA), 1x UART (low power) • Up to 2 SPI interfaces, up to 16 Mbits/s • 1x I2C (SMBus/PMBus)

• 8x timers: 1x 16-bit with up to 4 channels, 2x 16-bit with up to 2 channels, 1x 16-bit ultra-low-power timer, 1x SysTick, 1x RTC and 2x watchdogs (independent/window)

• CRC calculation unit, 96-bit unique ID

• All packages are ECOPACK®2

**Table 1. Device summary**

– PLL for CPU clock

• Pre-programmed bootloader

– USART, SPI supported

• Development support

– Serial wire debug supported

• Up to 38 fast I/Os (31 I/Os 5V tolerant) • Memories

– Up to 32-Kbyte Flash with ECC – 8-Kbyte RAM

– 1-Kbyte of data EEPROM with ECC – 20-byte backup register

– Sector protection against R/W operation

| **Reference** | **Part number** |
| --- | --- |
| STM32L031x4 | STM32L031G4, STM32L031K4, STM32L031C4, STM32L031E4, STM32L031F4 |
| STM32L031x6 | STM32L031G6, STM32L031K6, STM32L031C6, STM32L031E6, STM32L031F6 |

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This is information on a product in full production.

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**STM32L031x4/6 Introduction**

**1 Introduction**

The ultra-low-power STM32L031x4/6 family includes devices in 6 different packages from 20 to 48 pins. The description below gives an overview of the complete range of peripherals proposed in this family.

These features make the ultra-low-power STM32L031x4/6 microcontrollers suitable for a wide range of applications:

• Gas/water meters and industrial sensors

• Healthcare and fitness equipment

• Remote control and user interface

• PC peripherals, gaming, GPS equipment

• Alarm system, wired and wireless sensors, video intercom

This STM32L031x4/6 datasheet must be read in conjunction with the STM32L0x1 reference manual (RM0377).

For information on the Arm® Cortex®-M0+ core please refer to the Cortex®-M0+ Technical Reference Manual, available from the http://www.arm.com website.

*Figure 1* shows the general block diagram of the device family.

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**Description STM32L031x4/6**

**2 Description**

The access line ultra-low-power STM32L031x4/6 family incorporates the high-performance Arm® Cortex®-M0+ 32-bit RISC core operating at a 32 MHz frequency, high-speed embedded memories (up to 32 Kbytes of Flash program memory, 1 Kbytes of data EEPROM and 8 Kbytes of RAM) plus an extensive range of enhanced I/Os and peripherals.

The STM32L031x4/6 devices provide high power efficiency for a wide range of performance. It is achieved with a large choice of internal and external clock sources, an internal voltage adaptation and several low-power modes.

The STM32L031x4/6 devices offer several analog features, one 12-bit ADC with hardware oversampling, two ultra-low-power comparators, several timers, one low-power timer (LPTIM), three general-purpose 16-bit timers, one RTC and one SysTick which can be used as timebases. They also feature two watchdogs, one watchdog with independent clock and window capability and one window watchdog based on bus clock.

Moreover, the STM32L031x4/6 devices embed standard and advanced communication interfaces: one I2C, one SPI, one USART, and a low-power UART (LPUART).

The STM32L031x4/6 also include a real-time clock and a set of backup registers that remain powered in Standby mode.

The ultra-low-power STM32L031x4/6 devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. They are available in the -40 to +125 °C temperature range. A comprehensive set of power-saving modes allows the design of low-power applications.

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**STM32L031x4/6 Description**

**Figure 1. STM32L031x4/6 block diagram**

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**Description STM32L031x4/6**

**2.2 Ultra-low-power device continuum**

The ultra-low-power family offers a large choice of core and features, from 8-bit proprietary core up to Arm® Cortex®-M4, including Arm® Cortex®-M3 and Arm® Cortex®-M0+. The STM32Lx series are the best choice to answer your needs in terms of ultra-low-power features. The STM32 Ultra-low-power series are the best solution for applications such as gas/water meter, keyboard/mouse or fitness and healthcare application. Several built-in features like LCD drivers, dual-bank memory, low-power run mode, operational amplifiers, 128-bit AES, DAC, crystal-less USB and many other definitely help you building a highly cost optimized application by reducing BOM cost. STMicroelectronics, as a reliable and long-term manufacturer, ensures as much as possible pin-to-pin compatibility between all STM8Lx and STM32Lx on one hand, and between all STM32Lx and STM32Fx on the other hand. Thanks to this unprecedented scalability, your legacy application can be upgraded to respond to the latest market feature and efficiency requirements.

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**STM32L031x4/6 Functional overview**

**3 Functional overview**

**3.1 Low-power modes**

The ultra-low-power STM32L031x4/6 supports dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system’s maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

• Range 1 (VDD range limited to 1.71-3.6 V), with the CPU running at up to 32 MHz • Range 2 (full VDD range), with a maximum CPU frequency of 16 MHz

• Range 3 (full VDD range), with a maximum CPU frequency limited to 4.2 MHz Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

• **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.

• **Low-power run mode**

This mode is achieved with the multispeed internal (MSI) RC oscillator set to the low speed clock (max 131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In Low power run mode, the clock frequency and the number of enabled peripherals are both limited.

• **Low-power sleep mode**

This mode is achieved by entering Sleep mode with the internal voltage regulator in low-power mode to minimize the regulator’s operating current. In Low-power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

When wakeup is triggered by an event or an interrupt, the system reverts to the Run mode with the regulator on.

• **Stop mode with RTC**

The Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the VCORE domain are stopped, the PLL, MSI RC, HSE and HSI RC oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

The device can be woken up from Stop mode by any of the EXTI line, in 3.5 µs, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event

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**Functional overview STM32L031x4/6**

(if internal reference voltage is on), it can be the RTC alarm/tamper/timestamp/wakeup events, the USART/I2C/LPUART/LPTIMER wakeup events.

• **Stop mode without RTC**

The Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are disabled.

Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 3.5 µs, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on). It can also be wakened by the USART/I2C/LPUART/LPTIMER wakeup events.

• **Standby mode with RTC**

The Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire VCORE domain is powered off. The PLL, MSI RC, HSE and HSI RC oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC\_CSR register).

The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

• **Standby mode without RTC**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire VCORE domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC\_CSR register).

The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

*Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode.*

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**STM32L031x4/6 Functional overview**

**Table 3. Functionalities depending on the operating power supply range**

| **Operating power supply range(1)** | **Functionalities depending on the operating power supply range** | |
| --- | --- | --- |
| **ADC operation** | **Dynamic voltage scaling range** |
| VDD = 1.65 to 1.71 V | Conversion time up to 570 ksps | Range 2 or  range 3 |
| VDD = 1.71 to 2.0 V(2) | Conversion time up to 1.14 Msps | Range 1, range 2 or range 3 |
| VDD = 2.0 to 2.4 V | Conversion time up to 1.14 Msps | Range 1, range 2 or range 3 |
| VDD = 2.4 to 3.6 V | Conversion time up to 1.14 Msps | Range 1, range 2 or range 3 |

1. GPIO speed depends on VDD voltage range. Refer to *Table 55: I/O AC characteristics* for more information about I/O speed.

2. CPU frequency changes from initial to final must respect the condition: fCPU initial <4fCPU initial. It must also respect 5 μs delay between two changes. For example to switch from 4.2 MHz to 32 MHz, you can switch from 4.2 MHz to 16 MHz, wait 5 μs, then switch from 16 MHz to 32 MHz.

**Table 4. CPU frequency range depending on dynamic voltage scaling**

| **CPU frequency range** | **Dynamic voltage scaling range** |
| --- | --- |
| 16 MHz to 32 MHz (1ws)  32 kHz to 16 MHz (0ws) | Range 1 |
| 8 MHz to 16 MHz (1ws)  32 kHz to 8 MHz (0ws) | Range 2 |
| 32 kHz to 4.2 MHz (0ws) | Range 3 |

**Table 5. Functionalities depending on the working mode**

**(from Run/active down to standby) (1)**

| **IPs** | **Run/Active** | **Sleep** | **Low**  **power**  **run** | **Low**  **power**  **sleep** |  | **Stop** |  | **Standby** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Wakeup**  **capability** |  | **Wakeup**  **capability** |
| CPU | Y | -- | Y | -- | -- |  | -- |  |
| Flash memory | O | O | O | O | -- |  | -- |  |
| RAM | Y | Y | Y | Y | Y |  | -- |  |
| Backup registers | Y | Y | Y | Y | Y |  | Y |  |
| EEPROM | O | O | O | O | -- |  | -- |  |
| Brown-out reset (BOR) | O | O | O | O | O | O | O | O |
| DMA | O | O | O | O | -- |  | -- |  |

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**Functional overview STM32L031x4/6**

**Table 5. Functionalities depending on the working mode**

**(from Run/active down to standby) (continued)(1)**

| **IPs** | **Run/Active** | **Sleep** | **Low**  **power**  **run** | **Low**  **power**  **sleep** |  | **Stop** |  | **Standby** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Wakeup**  **capability** |  | **Wakeup**  **capability** |
| Programmable  voltage detector (PVD) | O | O | O | O | O | O | - |  |
| Power-on/down reset (POR/PDR) | Y | Y | Y | Y | Y | Y | Y | Y |
| High Speed  Internal (HSI) | O | O | -- | -- | (2) |  | -- |  |
| High Speed  External (HSE) | O | O | O | O | -- |  | -- |  |
| Low Speed Internal (LSI) | O | O | O | O | O |  | O |  |
| Low Speed  External (LSE) | O | O | O | O | O |  | O |  |
| Multi-Speed  Internal (MSI) | O | O | Y | Y | -- |  | -- |  |
| Inter-Connect  Controller | Y | Y | Y | Y | Y |  | -- |  |
| RTC | O | O | O | O | O | O | O |  |
| RTC Tamper | O | O | O | O | O | O | O | O |
| Auto WakeUp  (AWU) | O | O | O | O | O | O | O | O |
| USART | O | O | O | O | O(3) | O | -- |  |
| LPUART | O | O | O | O | O(3) | O | -- |  |
| SPI | O | O | O | O | -- |  | -- |  |
| I2C | O | O | -- | -- | O(4) | O | -- |  |
| ADC | O | O | -- | -- | -- |  | -- |  |
| Temperature  sensor | O | O | O | O | O |  | -- |  |
| Comparators | O | O | O | O | O | O | -- |  |
| 16-bit timers | O | O | O | O | -- |  | -- |  |
| LPTIMER | O | O | O | O | O | O |  |  |
| IWDG | O | O | O | O | O | O | O | O |
| WWDG | O | O | O | O | -- |  | -- |  |
| SysTick Timer | O | O | O | O |  |  | -- |  |
| GPIOs | O | O | O | O | O | O |  | 2 pins |

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**STM32L031x4/6 Functional overview**

**Table 5. Functionalities depending on the working mode**

**(from Run/active down to standby) (continued)(1)**

| **IPs** | **Run/Active** | **Sleep** | **Low**  **power**  **run** | **Low**  **power**  **sleep** |  | **Stop** |  | **Standby** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Wakeup**  **capability** |  | **Wakeup**  **capability** |
| Wakeup time to Run mode | 0 µs | 0.36 µs | 3 µs | 32 µs | 3.5 µs | | 65 µs | |
| Consumption  VDD=1.8 to 3.6 V (Typ) | Down to  115 µA/MHz  (from Flash) | Down to  25 µA/MHz  (from Flash) | Down to 6.5 µA | Down to 3.2 µA | 0.35 µA (No  RTC) VDD=1.8 V | | 0.23 µA (No  RTC) VDD=1.8 V | |
| 0.6 µA (with  RTC) VDD=1.8 V | | 0.39 µA (with  RTC) VDD=1.8 V | |
| 0.38 µA (No  RTC) VDD=3.0 V | | 0.26 µA (No  RTC) VDD=3.0 V | |
| 0.8 µA (with  RTC) VDD=3.0 V | | 0.57 µA (with  RTC) VDD=3.0 V | |

1. Legend:

“Y” = Yes (enable).

“O” = Optional, can be enabled/disabled by software)

“-” = Not available

2. Some peripherals with wakeup from Stop capability can request HSI to be enabled. In this case, HSI is woken up by the peripheral, and only feeds the peripheral which requested it. HSI is automatically put off when the peripheral does not need it anymore.

3. UART and LPUART reception is functional in Stop mode. It generates a wakeup interrupt on Start.To generate a wakeup on address match or received frame event, the LPUART can run on LSE clock while the UART has to wake up or keep running the HSI clock.

4. I2C address detection is functional in Stop mode. It generates a wakeup interrupt in case of address match. It will wake up the HSI during reception.

**3.2 Interconnect matrix**

Several peripherals are directly interconnected. This allows autonomous communication between peripherals, thus saving CPU resources and power consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, Low-power run, Low-power sleep and Stop modes.

**Table 6. STM32L0xx peripherals interconnect matrix**

| **Interconnect source** | **Interconnect destination** | **Interconnect action** | **Run** | **Sleep** | **Low**  **power run** | **Low**  **power**  **sleep** | **Stop** |
| --- | --- | --- | --- | --- | --- | --- | --- |
| COMPx | TIM2,TIM21,  TIM22 | Timer input channel, trigger from analog  signals comparison | Y | Y | Y | Y | - |
| LPTIM | Timer input channel, trigger from analog  signals comparison | Y | Y | Y | Y | Y |
| TIMx | TIMx | Timer triggered by other timer | Y | Y | Y | Y | - |

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**Functional overview STM32L031x4/6**

**Table 6. STM32L0xx peripherals interconnect matrix (continued)**

| **Interconnect source** | **Interconnect destination** | **Interconnect action** | **Run** | **Sleep** | **Low**  **power run** | **Low**  **power**  **sleep** | **Stop** |
| --- | --- | --- | --- | --- | --- | --- | --- |
| RTC | TIM21 | Timer triggered by Auto wake-up | Y | Y | Y | Y | - |
| LPTIM | Timer triggered by RTC event | Y | Y | Y | Y | Y |
| All clock  source | TIMx | Clock source used as input channel for RC measurement and  trimming | Y | Y | Y | Y | - |
| GPIO | TIMx | Timer input channel and trigger | Y | Y | Y | Y | - |
| LPTIM | Timer input channel and trigger | Y | Y | Y | Y | Y |
| ADC | Conversion trigger | Y | Y | Y | Y | - |

**3.3 Arm® Cortex®-M0+ core**

The Cortex-M0+ processor is an entry-level 32-bit Arm Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including: • a simple architecture that is easy to learn and program

• ultra-low power, energy-efficient operation

• excellent code density

• deterministic, high-performance interrupt handling

• upward compatibility with Cortex-M processor family

• platform security robustness.

The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32- bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

Owing to its embedded Arm core, the STM32L031x4/6 are compatible with all Arm tools and software.

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**STM32L031x4/6 Functional overview**

**Nested vectored interrupt controller (NVIC)**

The ultra-low-power STM32L031x4/6 embed a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels and 4 priority levels.

The Cortex-M0+ processor closely integrates a configurable Nested Vectored Interrupt Controller (NVIC), to deliver industry-leading interrupt performance. The NVIC: • includes a Non-Maskable Interrupt (NMI)

• provides zero jitter interrupt option

• provides four interrupt priority levels

The tight integration of the processor core and NVIC provides fast execution of Interrupt Service Routines (ISRs), dramatically reducing the interrupt latency. This is achieved through the hardware stacking of registers, and the ability to abandon and restart load multiple and store-multiple operations. Interrupt handlers do not require any assembler wrapper code, removing any code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with the sleep modes, that include a deep sleep function that enables the entire device to enter rapidly stop or standby mode.

This hardware block provides flexible interrupt management features with minimal interrupt latency.

**3.4 Reset and supply management**

**3.4.1 Power supply schemes**

• VDD = 1.65 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through VDD pins.

• VSSA, VDDA = 1.65 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL. VDDA and VSSA must be connected to VDD and VSS, respectively.

**3.4.2 Power supply supervisor**

The devices feature an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

Two versions are available:

• The version with BOR activated at power-on operates between 1.8 V and 3.6 V. • The other version without BOR operates between 1.65 V and 3.6 V.

After the VDD threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the VDD min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the power ramp-up must guarantee that 1.65 V is reached on VDD at least 1 ms after it exits the POR area.

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the

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**Functional overview STM32L031x4/6**

internal reference voltage (VREFINT) in Stop mode. The device remains in reset mode when VDD is below a specified threshold, VPOR/PDR or VBOR, without the need for any external reset circuit.

*Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.*

The devices feature an embedded programmable voltage detector (PVD) that monitors the VDD/VDDA power supply and compares it to the VPVD threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when VDD/VDDA drops below the VPVD threshold and/or when VDD/VDDA is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

**3.4.3 Voltage regulator**

The regulator has three operation modes: main (MR), low power (LPR) and power down. • MR is used in Run mode (nominal regulation)

• LPR is used in the Low-power run, Low-power sleep and Stop modes

• Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32 KHz oscillator, RCC\_CSR).

**3.4.4 Boot modes**

At startup, BOOT0 pin and nBOOT1 option bit are used to select one of three boot options: • Boot from Flash memory

• Boot from System memory

• Boot from embedded RAM

The boot loader is located in System memory. It is used to reprogram the Flash memory by using SPI1 (PA4, PA5, PA6, PA7), USART2 (PA2, PA3) or USART2 (PA9, PA10). See STM32™ microcontroller system memory boot mode AN2606 for details.

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**STM32L031x4/6 Functional overview**

**3.5 Clock management**

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

• **Clock prescaler**

To get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.

• **Safe clock switching**

Clock sources can be changed safely on the fly in Run mode through a configuration register.

• **Clock management**

To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.

• **System clock source**

Three different clock sources can be used to drive the master clock SYSCLK:

– 1-25 MHz high-speed external (HSE), that can supply a PLL

– 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL

– Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz). When a 32.768 kHz clock source is available in the system (LSE), the MSI

frequency can be trimmed by software down to a ±0.5% accuracy.

• **Auxiliary clock source**

Two ultra-low-power clock sources that can be used to drive the real-time clock: – 32.768 kHz low-speed external crystal (LSE)

– 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.

• **RTC clock sources**

The LSI, LSE or HSE sources can be chosen to clock the RTC, whatever the system clock.

• **Startup clock**

After reset, the microcontroller restarts by default with an internal 2 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.

• **Clock security system (CSS)**

This feature can be enabled by software. If an HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled. Another clock security system can be enabled, in case of failure of the LSE it provides an interrupt or wakeup event which is generated if enabled.

• **Clock-out capability (MCO: microcontroller clock output)**

It outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

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**Figure 2. Clock tree**

| #9  (QDEOH :DWFKGRJ  :DWFKGRJ /6 /6, 5&  /HJHQG  ~~/6, WHPSR~~  +6( +LJK VSHHG H[WHUQDO FORFN VLJQDO  +6, +LJK VSHHG LQWHUQDO FORFN VLJQDO  57&6(/  /6, /RZ VSHHG LQWHUQDO FORFN VLJQDO  57& HQDEOH  /6( /RZ VSHHG H[WHUQDO FORFN VLJQDO  06, 0XOWLVSHHG LQWHUQDO FORFN VLJQDO  /6( 26& 57&  ~~/6( WHPSR~~  /68 /6' /6'  #9  0+]  0&26(/  #9  $'& HQDEOH  /6,  06, 5&  $'&&/.  /6(  06,  /HYHO VKLIWHUV  0&2    #9  QRW GHHSVOHHS    &.B3:5  #9  QRW GHHSVOHHS  +6, 5&  FNBUFKV +6,  )&/.  /HYHO VKLIWHUV  QRW  VOHHS RU  GHHSVOHHS  #9  6\VWHP  &ORFN  +&/.  QRW  VOHHS RU  GHHSVOHHS    06,  7,0[&/.  #9  +6,  $+%  +6( 26&  ~~35(6&~~  +6(  3&/. WR $3%  «  /HYHO VKLIWHUV  SHULSKHUDOV  3//65&  3//&/.  $3%  #9  #9  35(6&  FNBSOOLQ  3//    /68  ;  3HULSKHUDO  #9    FORFN HQDEOH  WR 7,0[    0+] &ORFN  ,I  $3% SUHVF [    HOVH [  'HWHFWRU  /HYHO VKLIWHUV  3HULSKHUDO  #9''&25(  FORFN HQDEOH  &ORFN  +6( SUHVHQW RU QRW  /6'  3&/. WR $3%  6RXUFH  SHULSKHUDOV  0+]  $3%  PD[  &RQWURO  35(6&    3HULSKHUDO  FORFN HQDEOH  WR 7,0[  ,I  $3% SUHVF [  HOVH [  3HULSKHUDOV  /6,  HQDEOH  /37,0&/.  /6(  3HULSKHUDOV  HQDEOH  +6,  6<6&/.  /38$57  3&/.  3HULSKHUDOV  8$57&/.  HQDEOH  , & &/.  06Y 9 |
| --- |

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**STM32L031x4/6 Functional overview**

**3.6 Low-power real-time clock and backup registers**

The real time clock (RTC) and the 5 backup registers are supplied in all modes including standby mode. The backup registers are five 32-bit registers used to store 20 bytes of user application data. They are not reset by a system reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following: • Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format

• Automatically correction for 28, 29 (leap year), 30, and 31 day of the month • Two programmable alarms with wake up from Stop and Standby mode capability • Periodic wakeup from Stop and Standby with programmable resolution and period • On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.

• Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.

• Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy

• 2 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.

• Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

The RTC clock sources can be:

• A 32.768 kHz external crystal

• A resonator or oscillator

• The internal low-power RC oscillator (typical frequency of 37 kHz)

• The high-speed external clock

**3.7 General-purpose inputs/outputs (GPIOs)**

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated alternate function registers. All GPIOs are high current capable. Each GPIO output, speed can be slowed (40 MHz, 10 MHz, 2 MHz, 400 kHz). The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to a dedicated IO bus with a toggling speed of up to 32 MHz.

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**Functional overview STM32L031x4/6**

**3.8 Extended interrupt/event controller (EXTI)**

The extended interrupt/event controller consists of 26 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 38 GPIOs can be connected to the 16 configurable interrupt/event lines. The 10 other lines are connected to PVD, RTC, USART, I2C, LPUART, LPTIMER or comparator events.

**3.9 Memories**

The STM32L031x4/6 devices have the following features:

• 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses). • The non-volatile memory is divided into three arrays:

– 16 or 32 Kbytes of embedded Flash program memory

– 1 Kbytes of data EEPROM

– Information block containing 32 user and factory options bytes plus 4 Kbytes of system memory

The user options bytes are used to write-protect or read-out protect the memory (with 4- Kbyte granularity) and/or readout-protect the whole memory with the following options: • **Level 0**: no protection

• **Level 1**: memory readout protected.

The Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected

• **Level 2**: chip readout protected, debug features (Cortex-M0+ serial wire) and boot in RAM selection disabled (debugline fuse)

The whole non-volatile memory embeds the error correction code (ECC) feature.

**3.10 Direct memory access (DMA)**

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I2C, USART, LPUART,

general-purpose timers, and ADC.

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**3.11 Analog-to-digital converter (ADC)**

A native 12-bit, extended to 16-bit through hardware oversampling, analog-to-digital converter is embedded into STM32L031x4/6 devices. It has up to 10 external channels and 3 internal channels (temperature sensor, voltage reference). Three channel are fast channel, PA0, PA4 and PA5, while the others are standard channels.

It performs conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC frequency is independent from the CPU frequency, allowing maximum sampling rate of 1.14 Msps even with a low CPU speed. The ADC consumption is low at all frequencies (~25 µA at 10 kSPS, ~200 µA at 1 Msps). An auto-shutdown function guarantees that the ADC is powered off except during the active conversion phase.

The ADC can be served by the DMA controller. It can operate from a supply voltage down to 1.65 V.

The ADC features a hardware oversampler up to 256 samples, this improves the resolution to 16 bits (see AN2668).

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions and timers.

**3.12 Temperature sensor**

The temperature sensor (TSENSE) generates a voltage VSENSE that varies linearly with temperature.

The temperature sensor is internally connected to the ADC\_IN18 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

**Table 7. Temperature sensor calibration values**

| **Calibration value name** | **Description** | **Memory address** |
| --- | --- | --- |
| TSENSE\_CAL1 | TS ADC raw data acquired at temperature of 30 °C, VDDA= 3 V | 0x1FF8 007A - 0x1FF8 007B |
| TSENSE\_CAL2 | TS ADC raw data acquired at temperature of 130 °C, VDDA= 3 V | 0x1FF8 007E - 0x1FF8 007F |

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**Functional overview STM32L031x4/6**

**3.12.1 Internal voltage reference (VREFINT)**

The internal voltage reference (VREFINT) provides a stable (bandgap) voltage output for the ADC and Comparators. VREFINT is internally connected to the ADC\_IN17 input channel. It enables accurate monitoring of the VDD value (since no external voltage, VREF+, is available for ADC). The precise voltage of VREFINT is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

**Table 8. Internal voltage reference measured values**

| **Calibration value name** | **Description** | **Memory address** |
| --- | --- | --- |
| VREFINT\_CAL | Raw data acquired at  temperature of 25 °C  VDDA = 3 V | 0x1FF8 0078 - 0x1FF8 0079 |

**3.13 Ultra-low-power comparators and reference voltage**

The STM32L031x4/6 embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O). • One comparator with ultra low consumption

• One comparator with rail-to-rail inputs, fast or slow mode.

• The threshold can be one of the following:

– External I/O pins

– Internal reference voltage (VREFINT)

– submultiple of Internal reference voltage(1/4, 1/2, 3/4) for the rail to rail

comparator.

Both comparators can wake up the devices from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 µA typical).

**3.14 System configuration controller**

The system configuration controller provides the capability to remap some alternate functions on different I/O ports.

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM21, TIM22 and LPTIM timer input captures. It also controls the routing of internal analog signals to the ADC, COMP1 and COMP2 and the internal reference voltage VREFINT.

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**STM32L031x4/6 Functional overview**

**3.15 Timers and watchdogs**

The ultra-low-power STM32L031x4/6 devices include three general-purpose timers, one low- power timer (LPTM), two watchdog timers and the SysTick timer.

*Table 9* compares the features of the general-purpose and basic timers.

**Table 9. Timer feature comparison**

| **Timer** | **Counter**  **resolution** | **Counter type** | **Prescaler factor** | **DMA**  **request**  **generation** | **Capture/compare channels** | **Complementary outputs** |
| --- | --- | --- | --- | --- | --- | --- |
| TIM2 | 16-bit | Up, down,  up/down | Any integer between 1 and 65536 | Yes | 4 | No |
| TIM21, TIM22 | 16-bit | Up, down,  up/down | Any integer between 1 and 65536 | No | 2 | No |

**3.15.1 General-purpose timers (TIM2, TIM21 and TIM22)**

There are three synchronizable general-purpose timers embedded in the STM32L031x4/6 devices (see *Table 9* for differences).

**TIM2**

TIM2 is based on 16-bit auto-reload up/down counter. It includes a 16-bit prescaler. It features four independent channels each for input capture/output compare, PWM or one pulse mode output.

The TIM2 general-purpose timers can work together or with the TIM21 and TIM22 general purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2 has independent DMA request generation.

This timer is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

**TIM21 and TIM22**

TIM21 and TIM22 are based on a 16-bit auto-reload up/down counter. They include a 16-bit prescaler. They have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together and be synchronized with the TIM2, full featured general-purpose timers.

They can also be used as simple time bases and be clocked by the LSE clock source (32.768 kHz) to provide time bases independent from the main CPU clock.

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**Functional overview STM32L031x4/6**

**3.15.2 Low-power timer (LPTIM)**

The low-power timer has an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the devices from Stop mode.

This low-power timer supports the following features:

• 16-bit up counter with 16-bit autoreload register

• 16-bit compare register

• Configurable output: pulse, PWM

• Continuous / one shot mode

• Selectable software / hardware input trigger

• Selectable clock source

– Internal clock source: LSE, LSI, HSI or APB clock

– External clock source over LPTIM input (working even with no internal clock source running, used by the Pulse Counter Application)

• Programmable digital glitch filter

• Encoder mode

**3.15.3 SysTick timer**

This timer is dedicated to the OS, but could also be used as a standard downcounter. It is based on a 24-bit downcounter with autoreload capability and a programmable clock source. It features a maskable system interrupt generation when the counter reaches ‘0’.

**3.15.4 Independent watchdog (IWDG)**

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 37 kHz internal RC and, as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

**3.15.5 Window watchdog (WWDG)**

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

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**3.16 Communication interfaces**

**3.16.1 I2C bus**

One I2C interface (I2C1) can operate in multimaster or slave modes. The I2C interface can support Standard mode (Sm, up to 100 kbit/s), Fast mode (Fm, up to 400 kbit/s) and Fast Mode Plus (Fm+, up to 1 Mbit/s) with 20 mA output drive on some I/Os.

The I2C interface supports 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

**Table 10. Comparison of I2C analog and digital filters**

|  | **Analog filter** | **Digital filter** |
| --- | --- | --- |
| Pulse width of  suppressed spikes | ≥ 50 ns | Programmable length from 1 to 15 I2C peripheral clocks |
| Benefits | Available in Stop mode | 1. Extra filtering capability vs. standard requirements.  2. Stable length |
| Drawbacks | Variations depending on  temperature, voltage, process | Wakeup from Stop on address match is not available when digital filter is enabled. |

In addition, I2C1 provides hardware support for SMBus 2.0 and PMBus 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I2C interface can be served by the DMA controller.

Refer to *Table 11* for the supported modes and features of I2C interface.

**Table 11. STM32L031x4/6 I2C implementation**

| **I2C features(1)** | **I2C1** |
| --- | --- |
| 7-bit addressing mode | X |
| 10-bit addressing mode | X |
| Standard mode (up to 100 kbit/s) | X |
| Fast mode (up to 400 kbit/s) | X |
| Fast Mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s) | X(2) |
| Independent clock | X |
| SMBus | X |
| Wakeup from STOP | X |

1. X = supported.

2. See *Table 15: Pin definitions on page 39* for the list of I/Os that feature Fast Mode Plus capability DS10668 Rev 6 31/126

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**3.16.2 Universal synchronous/asynchronous receiver transmitter (USART)** The USART interface (USART2) is able to communicate at speeds of up to 4 Mbit/s.

it provides hardware management of the CTS, RTS and RS485 driver enable (DE) signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART2 also supports Smartcard communication (ISO

7816), IrDA SIR ENDEC, LIN Master/Slave capability, auto baud rate feature and has a clock domain independent from the CPU clock that allows to wake up the MCU from Stop mode using baudrates up to 42 Kbaud.

USART2 interface can be served by the DMA controller.

*Table 12* for the supported modes and features of USART interface.

**Table 12. USART implementation**

| **USART modes/features(1)** | **USART2** |
| --- | --- |
| Hardware flow control for modem | X |
| Continuous communication using DMA | X |
| Multiprocessor communication | X |
| Synchronous mode(2) | X |
| Smartcard mode | X |
| Single-wire half-duplex communication | X |
| IrDA SIR ENDEC block | X |
| LIN mode | X |
| Dual clock domain and wakeup from Stop mode | X |
| Receiver timeout interrupt | X |
| Modbus communication | X |
| Auto baud rate detection (4 modes) | X |
| Driver Enable | X |

1. X = supported.

2. This mode allows using the USART as an SPI master.

**3.16.3 Low-power universal asynchronous receiver transmitter (LPUART)**

The devices embed one Low-power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor

communication.

The LPUART has a clock domain independent from the CPU clock, and can wake up the system from Stop mode using baudrates up to 46 Kbaud. The Wakeup events from Stop mode are programmable and can be:

• Start bit detection

• Or any received data frame

• Or a specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while

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having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

LPUART interface can be served by the DMA controller.

**3.16.4 Serial peripheral interface (SPI)**

The SPI is able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The USARTs with synchronous capability can also be used as SPI master.

The SPI can be served by the DMA controller.

Refer to *Table 13* for the supported modes and features of SPI interface.

**Table 13. SPI implementation**

| **SPI features(1)** | **SPI1** |
| --- | --- |
| Hardware CRC calculation | X |
| I2S mode | - |
| TI mode | X |

1. X = supported.

**3.17 Cyclic redundancy check (CRC) calculation unit**

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

**3.18 Serial wire debug port (SW-DP)**

An Arm SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

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**Pin descriptions STM32L031x4/6**

**4 Pin descriptions**

**Figure 3. STM32L031x4/6 UFQFPN48**

| 7            6    '        2      %  %  %  6  %  $  $  %  2  %  %  '  3  3  3  3  3  9  3  3  %  3  3  9      3&  9''    966    3&    3& 26& B,1  3$      3$  3& 26& B287      3$    3+ 26&B,1    3$  3+ 26&B287      966  3$  1567        966$  3$  9''$    3%  3$      3%    3%  3$  3%  3$                                6  '      %  %  %  $  $  $  $  $  6  '  %  %  3  3  3  3  3  3  3  3  9  9  3  3  06Y 9 |
| --- |

1. The above figure shows the package top view.

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**STM32L031x4/6 Pin descriptions**

**Figure 4. STM32L031x4/6 LQFP48**

| 7                                  2                6      '  '  6  %  %  2  %  %  %  %  %  $  $  9  9  3  3  %  3  3  3  3  3  3  3      9''      3&  966  3&      3$  3& 26& B,1      3$  3& 26& B287      3$  3+ 26&B,1      3$    3+ 26&B287    /4)3  3$    1567    3$    966$    3%    9''$    3%    3$    3%    3$    3$  3%                              6  '      %  %  %  $  $  $  $  $  6  '  %  %  3  3  3  3  3  3  3  3  9  9  3  3  06Y 9 |
| --- |

1. The above figure shows the package bump view.

**Figure 5. STM32L031x4/6 LQFP32 pinout**

| 7    6            2    6  %  %  %  %  %  2  $  9  3  3  3  3  3  3  %    9''  3$      3$  3& 26&B,1      3$  3$ 26& B287      3$  /4)3  1567    3$      9''$    3$    3$ &.B,1    3$    3$    9''  3$                  6  %  %  $  $  $  $  $  6  3  3  3  3  3  3  3  9  06Y 9 |
| --- |

1. The above figure shows the package top view.

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**Pin descriptions STM32L031x4/6**

**Figure 6. STM32L031x4/6 UFQFPN32 pinout**

| 7      2              2  %  %  %  %  %  %  $  %  3  3  3  3  3  3  3    3$  9''    3$  3& 26& B,1      3& 26& B287  3$      3$  1567 966    3$  9''$      3$  3$ &.B,1      3$  3$        9''  3$                  %  %  %  $  $  $  $  $  3  3  3  3  3  3  3  3  06Y 9 |
| --- |

1. The above figure shows the package top view.

**Figure 7. STM32L031x4/6 UFQFPN28 pinout**

| 7      2  6            2  6  %  %  %  $  $  %  9  3  3  3  3  3        9''  3$      3& 26& B,1  3$      3$  3& 26& B287  1567  3$      9''$  9''      3$ &.B,1  966      3$  3%                          %  $  $  $  $  $  $  3  3  3  3  3  3  3  06Y 9 |
| --- |

1. The above figure shows the package top view.

2. This pinout applies to all part numbers except for STM32L031GxUxS .

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**STM32L031x4/6 Pin descriptions**

**Figure 8. STM32L031 UFQFPN28 pinout**

| %  %  %  %  %  $  $  3  3  3  3  3  3  3        %227  3$      3& 26& B,1  3$      3$  3& 26& B287    1567  3$    9''$  9''      3$ &.B,1  966      3$  3%                          %  $  $  $  $  $  $  3  3  3  3  3  3  3  06Y 9 |
| --- |

1. The above figure shows the package top view.

2. This pinout applies only to STM32L031GxUxS part number.

**Figure 9. STM32L031x4/6 TSSOP20 pinout**

| %227  3$      3& 26& B,1  3$      3& 26& B287  3$      1567  3$      9''$  9''      3$ &.B,1  966      3$  3%      3$  3$      3$      3$  3$  3$    06Y 9 |
| --- |

1. The above figure shows the package top view.

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**Pin descriptions STM32L031x4/6**

**Figure 10. STM32L031x4/6 WLCSP25 pinout**

| $  3$  3% 3% %227  3$  3&  %  3$ 3$  26& B  3$  3%  ,1  3&  26&  3$  3$  &  3$ 9''$  B287  '  9''  3%  3$ 3$ 1567  3$ 3$ 3$  3%  (  966$  &.B,1  06Y 9 |
| --- |

1. The above figure shows the package top view.

**Table 14. Legend/abbreviations used in the pinout table**

| **Name** | | **Abbreviation** | **Definition** |
| --- | --- | --- | --- |
| Pin name | | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name | |
| Pin type | | S | Supply pin |
| I | Input only pin |
| I/O | Input / output pin |
| I/O structure | | FT | 5 V tolerant I/O |
| FTf | 5 V tolerant I/O, FM+ capable |
| TC | Standard 3.3V I/O |
| B | Dedicated BOOT0 pin |
| RST | Bidirectional reset pin with embedded weak pull-up resistor |
| Notes | | Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset. | |
| Pin functions | Alternate  functions | Functions selected through GPIOx\_AFR registers | |
| Additional functions | Functions directly selected/enabled through peripheral registers | |

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**STM32L031x4/6 Pin descriptions**

**Table 15. Pin definitions**

| **Pin Number** | | | | | | | | **Pin name**  **(function**  **after reset)** | **Pin**  **type** | **e**  **r**  **u**  **t**  **c**  **u**  **r**  **t**  **s**    **O**  **/**  **I** | **e**  **t**  **o**  **N** | **Alternate**  **functions** | **Additional functions** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **0**  **2**  **P**  **O**  **S**  **S**  **T** | **5**  **2**  **P**  **S**  **C**  **L**  **W** | **8**  **2**  **N**  **P**  **F**  **Q**  **F**  **U** | **)**  **y**  **l**  **n**  **o**    **S**  **x**  **U**  **x**  **G**  **1**  **3**  **0**  **L**  **2**  **3**  **M**  **T**  **S**  **(**    **8**  **2**  **N**  **P**  **F**  **Q**  **F**  **U** | **2**  **3**  **P**  **F**  **Q**  **L** | **)**  **1**  **(**  **2**  **3**  **N**  **P**  **F**  **Q**  **F**  **U** | **8**  **4**  **P**  **F**  **Q**  **L** | **8**  **4**  **N**  **P**  **F**  **Q**  **F**  **U** |
| - | - | - | - | - | - | 2 | 2 | PC13-  ANTI\_TAMP | I/O | FT | - | - | TAMP1/WKUP2 |
| 2 | B5 | 2 | 2 | 2 | 2 | 3 | 3 | PC14-  OSC32\_IN | I/O | TC | - | - | OSC32\_IN |
| 3 | C5 | 3 | 3 | 3 | 3 | 4 | 4 | PC15-  OSC32\_OU T | I/O | TC | - | - | OSC32\_OUT |
| - | - | - | - | - | - | 5 | 5 | PH0-  OSC\_IN | I/O | TC | - | - | - |
| - | - | - | - | - | - | 6 | 6 | PH1-  OSC\_OUT | I/O | TC | - | - | - |
| 4 | D5 | 4 | 4 | 4 | 4 | 7 | 7 | NRST | I/O | - | - | - | - |
| - | - | - | - | - | - | 1 | 1 | PC0 | I/O | FT | - | LPTIM1\_IN1, EVENTOUT,  LPUART1\_RX | - |
| - | E1 | - | - | - | "0" | 8 | 8 | VSSA | S | - | - | - | - |
| 5 | C4 | 5 | 5 | 5 | 5 | 9 | 9 | VDDA | S | - | - | - | - |
| 6 | E5 | 6 | 6 | 6 | 6 | - | - | PA0-CK\_IN | I/O | TC | - | LPTIM1\_IN1, TIM2\_CH1,  USART2\_CTS, TIM2\_ETR,  COMP1\_OUT | COMP1\_INM6,  ADC\_IN0,  RTC\_TAMP2/WKUP1 |
| - | - | - | - | - | - | 10 | 10 | PA0 | I/O | TC | - | LPTIM1\_IN1, TIM2\_CH1,  USART2\_CTS, TIM2\_ETR,  COMP1\_OUT | COMP1\_INM6,  ADC\_IN0,  RTC\_TAMP2/WKUP1 |

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**Pin descriptions STM32L031x4/6**

**Table 15. Pin definitions (continued)**

| **Pin Number** | | | | | | | | **Pin name**  **(function**  **after reset)** | **Pin**  **type** | **e**  **r**  **u**  **t**  **c**  **u**  **r**  **t**  **s**    **O**  **/**  **I** | **e**  **t**  **o**  **N** | **Alternate**  **functions** | **Additional functions** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **0**  **2**  **P**  **O**  **S**  **S**  **T** | **5**  **2**  **P**  **S**  **C**  **L**  **W** | **8**  **2**  **N**  **P**  **F**  **Q**  **F**  **U** | **)**  **y**  **l**  **n**  **o**    **S**  **x**  **U**  **x**  **G**  **1**  **3**  **0**  **L**  **2**  **3**  **M**  **T**  **S**  **(**    **8**  **2**  **N**  **P**  **F**  **Q**  **F**  **U** | **2**  **3**  **P**  **F**  **Q**  **L** | **)**  **1**  **(**  **2**  **3**  **N**  **P**  **F**  **Q**  **F**  **U** | **8**  **4**  **P**  **F**  **Q**  **L** | **8**  **4**  **N**  **P**  **F**  **Q**  **F**  **U** |
| 7 | B4 | 7 | 7 | 7 | 7 | 11 | 11 | PA1 | I/O | FT | - | EVENTOUT,  LPTIM1\_IN2, TIM2\_CH2,  I2C1\_SMBA,  USART2\_RTS/ USART2\_DE, TIM21\_ETR | COMP1\_INP,  ADC\_IN1 |
| 8 | D4 | 8 | 8 | 8 | 8 | 12 | 12 | PA2 | I/O | TC | - | TIM21\_CH1,  TIM2\_CH3,  USART2\_TX, LPUART1\_TX, COMP2\_OUT | COMP2\_INM6,  ADC\_IN2,  RTC\_TAMP3/RTC\_TS /RTC\_OUT/WKUP3 |
| 9 | E4 | 9 | 9 | 9 | 9 | 13 | 13 | PA3 | I/O | FT | - | TIM21\_CH2,  TIM2\_CH4,  USART2\_RX, LPUART1\_RX | COMP2\_INP,  ADC\_IN3 |
| 10 | B3 | 10 | 10 | 10 | 10 | 14 | 14 | PA4 | I/O | TC | - | SPI1\_NSS,  LPTIM1\_IN1, USART2\_CK, TIM22\_ETR | COMP1\_INM4,  COMP2\_INM4,  ADC\_IN4 |
| 11 | D3 | 11 | 11 | 11 | 11 | 15 | 15 | PA5 | I/O | TC | - | SPI1\_SCK,  LPTIM1\_IN2, TIM2\_ETR,  TIM2\_CH1 | COMP1\_INM5,  COMP2\_INM5,  ADC\_IN5 |
| 12 | E3 | 12 | 12 | 12 | 12 | 16 | 16 | PA6 | I/O | FT | - | SPI1\_MISO,  LPTIM1\_ETR, LPUART1\_CTS, TIM22\_CH1,  EVENTOUT,  COMP1\_OUT | ADC\_IN6 |

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**STM32L031x4/6 Pin descriptions**

**Table 15. Pin definitions (continued)**

| **Pin Number** | | | | | | | | **Pin name**  **(function**  **after reset)** | **Pin**  **type** | **e**  **r**  **u**  **t**  **c**  **u**  **r**  **t**  **s**    **O**  **/**  **I** | **e**  **t**  **o**  **N** | **Alternate**  **functions** | **Additional functions** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **0**  **2**  **P**  **O**  **S**  **S**  **T** | **5**  **2**  **P**  **S**  **C**  **L**  **W** | **8**  **2**  **N**  **P**  **F**  **Q**  **F**  **U** | **)**  **y**  **l**  **n**  **o**    **S**  **x**  **U**  **x**  **G**  **1**  **3**  **0**  **L**  **2**  **3**  **M**  **T**  **S**  **(**    **8**  **2**  **N**  **P**  **F**  **Q**  **F**  **U** | **2**  **3**  **P**  **F**  **Q**  **L** | **)**  **1**  **(**  **2**  **3**  **N**  **P**  **F**  **Q**  **F**  **U** | **8**  **4**  **P**  **F**  **Q**  **L** | **8**  **4**  **N**  **P**  **F**  **Q**  **F**  **U** |
| 13 | C3 | 13 | 13 | 13 | 13 | 17 | 17 | PA7 | I/O | FT | - | SPI1\_MOSI,  LPTIM1\_OUT, USART2\_CTS, TIM22\_CH2,  EVENTOUT,  COMP2\_OUT | ADC\_IN7 |
| - | E2 | 14 | 14 | 14 | 14 | 18 | 18 | PB0 | I/O | FT | - | EVENTOUT,  SPI1\_MISO,  USART2\_RTS/ USART2\_DE, TIM2\_CH3 | ADC\_IN8, VREF\_OUT |
| 14 | D2 | 15 | 15 | 15 | 15 | 19 | 19 | PB1 | I/O | FT | - | USART2\_CK, SPI1\_MOSI,  LPUART1\_RTS/ LPUART1\_DE, TIM2\_CH4 | ADC\_IN9, VREF\_OUT |
| - | - | - | - | - | 16 | 20 | 20 | PB2 | I/O | FT | - | LPTIM1\_OUT | - |
| - | - | - | - | - | - | 21 | 21 | PB10 | I/O | FT | - | TIM2\_CH3,  LPUART1\_TX | - |
| - | - | - | - | - | - | 22 | 22 | PB11 | I/O | FT | - | EVENTOUT,  TIM2\_CH4,  LPUART1\_RX | - |
| 15 | - | 16 | 16 | 16 | - | 23 | 23 | VSS | S | - | - | - | - |
| 16 | - | 17 | 17 | 17 | 17 | 24 | 24 | VDD | S | - | - | - | - |
| - | - | - | - | - | - | 25 | 25 | PB12 | I/O | FT | - | SPI1\_NSS,  EVENTOUT | - |

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**Pin descriptions STM32L031x4/6**

**Table 15. Pin definitions (continued)**

| **Pin Number** | | | | | | | | **Pin name**  **(function**  **after reset)** | **Pin**  **type** | **e**  **r**  **u**  **t**  **c**  **u**  **r**  **t**  **s**    **O**  **/**  **I** | **e**  **t**  **o**  **N** | **Alternate**  **functions** | **Additional functions** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **0**  **2**  **P**  **O**  **S**  **S**  **T** | **5**  **2**  **P**  **S**  **C**  **L**  **W** | **8**  **2**  **N**  **P**  **F**  **Q**  **F**  **U** | **)**  **y**  **l**  **n**  **o**    **S**  **x**  **U**  **x**  **G**  **1**  **3**  **0**  **L**  **2**  **3**  **M**  **T**  **S**  **(**    **8**  **2**  **N**  **P**  **F**  **Q**  **F**  **U** | **2**  **3**  **P**  **F**  **Q**  **L** | **)**  **1**  **(**  **2**  **3**  **N**  **P**  **F**  **Q**  **F**  **U** | **8**  **4**  **P**  **F**  **Q**  **L** | **8**  **4**  **N**  **P**  **F**  **Q**  **F**  **U** |
| - | - | - | - | - | - | 26 | 26 | PB13 | I/O | FT | - | SPI1\_SCK,  MCO,  TIM21\_CH1,  LPUART1\_CTS | - |
| - | - | - | - | - | - | 27 | 27 | PB14 | I/O | FT | - | SPI1\_MISO,  RTC\_OUT,  TIM21\_CH2,  LPUART1\_RTS/ LPUART1\_DE | - |
| - | - | - | - | - | - | 28 | 28 | PB15 | I/O | FT | - | SPI1\_MOSI,  RTC\_REFIN | - |
| - | C1 | 18 | 18 | 18 | 18 | 29 | 29 | PA8 | I/O | FT | - | MCO,  LPTIM1\_IN1, EVENTOUT,  USART2\_CK, TIM2\_CH1 | - |
| 17 | B1 | 19 | 19 | 19 | 19 | 30 | 30 | PA9 | I/O | FTf | - | MCO,  I2C1\_SCL,  USART2\_TX, TIM22\_CH1 | - |
| 18 | C2 | 20 | 20 | 20 | 20 | 31 | 31 | PA10 | I/O | FTf | - | I2C1\_SDA,  USART2\_RX, TIM22\_CH2 | - |
| - | - | - | - | 21 | 21 | 32 | 32 | PA11 | I/O | FT | - | SPI1\_MISO,  EVENTOUT,  USART2\_CTS, TIM21\_CH2,  COMP1\_OUT | - |

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**STM32L031x4/6 Pin descriptions**

**Table 15. Pin definitions (continued)**

| **Pin Number** | | | | | | | | **Pin name**  **(function**  **after reset)** | **Pin**  **type** | **e**  **r**  **u**  **t**  **c**  **u**  **r**  **t**  **s**    **O**  **/**  **I** | **e**  **t**  **o**  **N** | **Alternate**  **functions** | **Additional functions** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **0**  **2**  **P**  **O**  **S**  **S**  **T** | **5**  **2**  **P**  **S**  **C**  **L**  **W** | **8**  **2**  **N**  **P**  **F**  **Q**  **F**  **U** | **)**  **y**  **l**  **n**  **o**    **S**  **x**  **U**  **x**  **G**  **1**  **3**  **0**  **L**  **2**  **3**  **M**  **T**  **S**  **(**    **8**  **2**  **N**  **P**  **F**  **Q**  **F**  **U** | **2**  **3**  **P**  **F**  **Q**  **L** | **)**  **1**  **(**  **2**  **3**  **N**  **P**  **F**  **Q**  **F**  **U** | **8**  **4**  **P**  **F**  **Q**  **L** | **8**  **4**  **N**  **P**  **F**  **Q**  **F**  **U** |
| - | - | - | - | 22 | 22 | 33 | 33 | PA12 | I/O | FT | - | SPI1\_MOSI,  EVENTOUT,  USART2\_RTS/ USART2\_DE, COMP2\_OUT | - |
| 19 | A1 | 21 | 21 | 23 | 23 | 34 | 34 | PA13 | I/O | FT | - | SWDIO,  LPTIM1\_ETR, LPUART1\_RX | - |
| - | - | - | - | - | - | 35 | 35 | VSS | S | - | - | - | - |
| - | D1 | - | - | - | - | 36 | 36 | VDD | S | - | - | - | - |
| 20 | A2 | 22 | 22 | 24 | 24 | 37 | 37 | PA14 | I/O | FT | - | SWCLK,  LPTIM1\_OUT, I2C1\_SMBA,  USART2\_TX, LPUART1\_TX | - |
| - | - | 23 | 23 | 25 | 25 | 38 | 38 | PA15 | I/O | FT | - | SPI1\_NSS,  TIM2\_ETR,  EVENTOUT,  USART2\_RX, TIM2\_CH1 | -- |
| - | B2 | 24 | 24 | 26 | 26 | 39 | 39 | PB3 | I/O | FT | - | SPI1\_SCK,  TIM2\_CH2,  EVENTOUT | COMP2\_INN |
| - | - | - | 25 | 27 | 27 | 40 | 40 | PB4 | I/O | FT | - | SPI1\_MISO,  EVENTOUT,  TIM22\_CH1 | COMP2\_INP |

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**Pin descriptions STM32L031x4/6**

**Table 15. Pin definitions (continued)**

| **Pin Number** | | | | | | | | **Pin name**  **(function**  **after reset)** | **Pin**  **type** | **e**  **r**  **u**  **t**  **c**  **u**  **r**  **t**  **s**    **O**  **/**  **I** | **e**  **t**  **o**  **N** | **Alternate**  **functions** | **Additional functions** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **0**  **2**  **P**  **O**  **S**  **S**  **T** | **5**  **2**  **P**  **S**  **C**  **L**  **W** | **8**  **2**  **N**  **P**  **F**  **Q**  **F**  **U** | **)**  **y**  **l**  **n**  **o**    **S**  **x**  **U**  **x**  **G**  **1**  **3**  **0**  **L**  **2**  **3**  **M**  **T**  **S**  **(**    **8**  **2**  **N**  **P**  **F**  **Q**  **F**  **U** | **2**  **3**  **P**  **F**  **Q**  **L** | **)**  **1**  **(**  **2**  **3**  **N**  **P**  **F**  **Q**  **F**  **U** | **8**  **4**  **P**  **F**  **Q**  **L** | **8**  **4**  **N**  **P**  **F**  **Q**  **F**  **U** |
| - | - | - | 26 | 28 | 28 | 41 | 41 | PB5 | I/O | FT | - | SPI1\_MOSI,  LPTIM1\_IN1, I2C1\_SMBA,  TIM22\_CH2 | COMP2\_INP |
| - | A3 | 25 | 27 | 29 | 29 | 42 | 42 | PB6 | I/O | FTf | - | USART2\_TX, I2C1\_SCL,  LPTIM1\_ETR, TIM21\_CH1 | COMP2\_INP |
| - | A4 | 26 | 28 | 30 | 30 | 43 | 43 | PB7 | I/O | FTf | - | USART2\_RX, I2C1\_SDA,  LPTIM1\_IN2 | COMP2\_INP,  VREF\_PVD\_IN |
| 1 | A5 | 27 | 1 | 31 | 31 | 44 | 44 | BOOT0 | I | - | - | - | - |
| - | - | - | - | - | 32 | 45 | 45 | PB8 | I/O | FTf | - | I2C1\_SCL | - |
| - | - | - | - | - | - | 46 | 46 | PB9 | I/O | FTf | - | EVENTOUT,  I2C1\_SDA | - |
| - | - | 28 | - | 32 | - | 47 | 47 | VSS | S | - | - | - | - |
| - | - | 1 | - | 1 | 1 | 48 | 48 | VDD | S | - | - | - | - |

1. VSS pins are connected to the exposed pad (see *Figure 43: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline*).

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**STM32L031x4/6 Memory mapping**

**5 Memory mapping**

Refer to the product line reference manual for details on the memory mapping as well as the boundary addresses for all peripherals.

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**Electrical characteristics STM32L031x4/6 6 Electrical characteristics**

**6.1 Parameter conditions**

Unless otherwise specified, all voltages are referenced to VSS.

**6.1.1 Minimum and maximum values**

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at TA = 25 °C and TA = TAmax (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

**6.1.2 Typical values**

Unless otherwise specified, typical data are based on TA = 25 °C, VDD = 3.6 V (for the 1.65 V ≤ VDD ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

**6.1.3 Typical curves**

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

**6.1.4 Loading capacitor**

The loading conditions used for pin parameter measurement are shown in *Figure 11*.

**6.1.5 Pin input voltage**

The input voltage measurement on a pin of the device is described in *Figure 12*.

| **Figure 11. Pin loading conditions**  0&8 SLQ  & S)  DL F | **Figure 12. Pin input voltage**  0&8 SLQ  9,1  DL F |
| --- | --- |

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**STM32L031x4/6 Electrical characteristics**

**6.1.6 Power supply scheme**

**Figure 13. Power supply scheme**

| 6WDQGE\ SRZHU FLUFXLWU\  26& 57& :DNH XS  ORJLF 57& EDFNXS  UHJLVWHUV  287  U  H  ,2  W  I  L  \*3 , 2V  K  /RJLF  ,1 .HUQHO ORJLF  V    O  H  &38  Y  H  'LJLWDO  /  0HPRULHV  9''  9''  5HJXODWRU  1 î Q)  î )  966  9''$  9''$  $QDORJ  Q)  5& 3// &203  )  $'&  «  966$  06Y 9 |
| --- |

**6.1.7 Current consumption measurement**

**Figure 14. Current consumption measurement scheme**

| 9''$  ,''  1[9''  1 î Q)  î ) 1[966  06Y 9 |
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**Electrical characteristics STM32L031x4/6**

**6.2 Absolute maximum ratings**

Stresses above the absolute maximum ratings listed in *Table 17: Voltage characteristics*, *Table 18: Current characteristics*, and *Table 19: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard. Extended mission profiles are available on demand.

**Table 17. Voltage characteristics**

| **Symbol** | **Ratings** | **Min** | **Max** | **Unit** |
| --- | --- | --- | --- | --- |
| VDD–VSS | External main supply voltage  (including VDDA, VDD)(1) | –0.3 | 4.0 | V |
| VIN(2) | Input voltage on FT and FTf pins | VSS − 0.3 | VDD+4.0 |
| Input voltage on TC pins | VSS − 0.3 | 4.0 |
| Input voltage on BOOT0 | VSS | VDD +4.0 |
| Input voltage on any other pin | VSS −0.3 | 4.0 |
| |ΔVDD| | Variations between different VDDx power pins | - | 50 | mV |
| |VDDA-VDDx| | Variations between any VDDx and VDDA power pins(3) | - | 300 |
| |ΔVSS| | Variations between all different ground pins | - | 50 |
| VESD(HBM) | Electrostatic discharge voltage  (human body model) | see *Section 6.3.11* | |  |

1. All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.

2. VIN maximum must always be respected. Refer to *Table 18* for maximum allowed injected current values. 3. It is recommended to power VDD and VDDA from the same source. A maximum difference of 300 mV between VDD and VDDA can be tolerated during power-up and device operation.

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**STM32L031x4/6 Electrical characteristics**

**Table 18. Current characteristics**

| **Symbol** | **Ratings** | **Max.** | **Unit** |
| --- | --- | --- | --- |
| ΣIVDD(2) | Total current into sum of all VDD power lines (source)(1) | 105 | mA |
| ΣIVSS(2) | Total current out of sum of all VSS ground lines (sink)(1) | 105 |
| IVDD(PIN) | Maximum current into each VDD power pin (source)(1) | 100 |
| IVSS(PIN) | Maximum current out of each VSS ground pin (sink)(1) | 100 |
| IIO | Output current sunk by any I/O and control pin except FTf pins | 16 |
| Output current sunk by FTf pins | 22 |
| Output current sourced by any I/O and control pin | –16 |
| ΣIIO(PIN)(3) | Total output current sunk by sum of all IOs and control pins(4) | 45 |
| Total output current sourced by sum of all IOs and control pins(4) | -45 |
| ΣIIO(PIN)(5) | Total output current sunk by sum of all IOs and control pins(2) | 90 |
| Total output current sourced by sum of all IOs and control pins(2) | -90 |
| IINJ(PIN) | Injected current on FT, FFf, RST and B pins | –5/+0(6) |
| Injected current on TC pin | ± 5(7) |
| ΣIINJ(PIN) | Total injected current (sum of all I/O and control pins)(8) | ± 25 |

1. All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.

2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.

3. These values apply only to STM32L031GxUxS part number.

4. This current consumption must be correctly distributed over all I/Os and control pins. In particular, it must be located the closest possible to the couple of supply and ground, and distributed on both sides.

5. These values apply to all part numbers except for STM32L031GxUxS.

6. Positive current injection is not possible on these I/Os. A negative injection is induced by VIN<VSS. IINJ(PIN) must never be exceeded. Refer to *Table 17* for maximum allowed input voltage values.

7. A positive injection is induced by VIN > VDD while a negative injection is induced by VIN < VSS. IINJ(PIN) must never be exceeded. Refer to *Table 17: Voltage characteristics* for the maximum allowed input voltage values.

8. When several inputs are submitted to a current injection, the maximum ΣIINJ(PIN) is the absolute sum of the positive and negative injected currents (instantaneous values).

**Table 19. Thermal characteristics**

| **Symbol** | **Ratings** | **Value** | **Unit** |
| --- | --- | --- | --- |
| TSTG | Storage temperature range | –65 to +150 | °C |
| TJ | Maximum junction temperature | 150 | °C |

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**Electrical characteristics STM32L031x4/6 6.3 Operating conditions**

**6.3.1 General operating conditions**

**Table 20. General operating conditions**

| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| fHCLK | Internal AHB clock frequency | - | 0 | 32 | MHz |
| fPCLK1 | Internal APB1 clock frequency | - | 0 | 32 |
| fPCLK2 | Internal APB2 clock frequency | - | 0 | 32 |
| VDD | Standard operating voltage | BOR detector disabled | 1.65 | 3.6 | V |
| BOR detector enabled, at power on | 1.8 | 3.6 |
| BOR detector disabled, after power on | 1.65 | 3.6 |
| VDDA | Analog operating voltage  (all features) | Must be the same voltage as VDD(1) | 1.65 | 3.6 | V |
| VIN | Input voltage on FT, FTf and RST pins(2) | 2.0 V ≤ VDD ≤ 3.6 V | –0.3 | 5.5 | V |
| 1.65 V ≤ VDD ≤ 2.0 V | –0.3 | 5.2 |
| Input voltage on BOOT0 pin | - | 0 | 5.5 |
| Input voltage on TC pin | - | –0.3 | VDD+0.3 |
| PD | Power dissipation at TA = 85 °C (range 6) or TA =105 °C (rage 7) (3) | LQFP48 package | - | 351 | mW |
| UFQFPN48 package | - | 625 |
| LQFP32 package | - | 333 |
| UFQFPN32 package | - | 513 |
| UFQFPN28 package | - | 167 |
| WLCSP25 package | - | 286 |
| TSSOP20 package | - | 333 |
| Power dissipation at TA = 125 °C (range 3) (3) | LQFP48 package | - | 88 |
| UFQFPN48 package | - | 156 |
| LQFP32 package | - | 83 |
| UFQFPN32 package | - | 128 |
| UFQFPN28 package | - | 42 |
| WLCSP25 package | - | 71 |
| TSSOP20 package | - | 83 |

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**Table 20. General operating conditions (continued)**

| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| TA | Temperature range | Maximum power  dissipation (range 6) | –40 | 85 | °C |
| Maximum power  dissipation (range 7) | –40 | 105 |
| Maximum power  dissipation (range 3) | –40 | 125 |
| TJ | Junction temperature range (range 6) | -40 °C ≤ TA ≤ 85 °C | –40 | 105 |
| Junction temperature range (range 7) | -40 °C ≤ TA ≤ 105 °C | –40 | 125 |
| Junction temperature range (range 3) | -40 °C ≤ TA ≤ 125 °C | –40 | 130 |

1. It is recommended to power VDD and VDDA from the same source. A maximum difference of 300 mV between VDD and VDDA can be tolerated during power-up and normal operation.

2. To sustain a voltage higher than VDD+0.3V, the internal pull-up/pull-down resistors must be disabled. 3. If TA is lower, higher PD values are allowed as long as TJ does not exceed TJ max (see *Table 19: Thermal characteristics on page 51*).

**6.3.2 Embedded reset and power control block characteristics**

The parameters given in the following table are derived from the tests performed under the ambient temperature condition summarized in *Table 20*.

**Table 21. Embedded reset and power control block characteristics**

| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| --- | --- | --- | --- | --- | --- | --- |
| tVDD(1) | VDD rise time rate | BOR detector enabled | 0 | - | ∞ | µs/V |
| BOR detector disabled | 0 | - | 1000 |
| VDD fall time rate | BOR detector enabled | 20 | - | ∞ |
| BOR detector disabled | 0 | - | 1000 |
| TRSTTEMPO(1) | Reset temporization | VDD rising, BOR enabled | - | 2 | 3.3 | ms |
| VDD rising, BOR disabled(2) | 0.4 | 0.7 | 1.6 |
| VPOR/PDR | Power on/power down reset threshold | Falling edge | 1 | 1.5 | 1.65 | V |
| Rising edge | 1.3 | 1.5 | 1.65 |
| VBOR0 | Brown-out reset threshold 0 | Falling edge | 1.67 | 1.7 | 1.74 |
| Rising edge | 1.69 | 1.76 | 1.8 |
| VBOR1 | Brown-out reset threshold 1 | Falling edge | 1.87 | 1.93 | 1.97 |
| Rising edge | 1.96 | 2.03 | 2.07 |
| VBOR2 | Brown-out reset threshold 2 | Falling edge | 2.22 | 2.30 | 2.35 |
| Rising edge | 2.31 | 2.41 | 2.44 |

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**Electrical characteristics STM32L031x4/6**

**Table 21. Embedded reset and power control block characteristics (continued)**

| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| --- | --- | --- | --- | --- | --- | --- |
| VBOR3 | Brown-out reset threshold 3 | Falling edge | 2.45 | 2.55 | 2.6 | V |
| Rising edge | 2.54 | 2.66 | 2.7 |
| VBOR4 | Brown-out reset threshold 4 | Falling edge | 2.68 | 2.8 | 2.85 |
| Rising edge | 2.78 | 2.9 | 2.95 |
| VPVD0 | Programmable voltage detector threshold 0 | Falling edge | 1.8 | 1.85 | 1.88 |
| Rising edge | 1.88 | 1.94 | 1.99 |
| VPVD1 | PVD threshold 1 | Falling edge | 1.98 | 2.04 | 2.09 |
| Rising edge | 2.08 | 2.14 | 2.18 |
| VPVD2 | PVD threshold 2 | Falling edge | 2.20 | 2.24 | 2.28 |
| Rising edge | 2.28 | 2.34 | 2.38 |
| VPVD3 | PVD threshold 3 | Falling edge | 2.39 | 2.44 | 2.48 |
| Rising edge | 2.47 | 2.54 | 2.58 |
| VPVD4 | PVD threshold 4 | Falling edge | 2.57 | 2.64 | 2.69 |
| Rising edge | 2.68 | 2.74 | 2.79 |
| VPVD5 | PVD threshold 5 | Falling edge | 2.77 | 2.83 | 2.88 |
| Rising edge | 2.87 | 2.94 | 2.99 |
| VPVD6 | PVD threshold 6 | Falling edge | 2.97 | 3.05 | 3.09 |
| Rising edge | 3.08 | 3.15 | 3.20 |
| Vhyst | Hysteresis voltage | BOR0 threshold | - | 40 | - | mV |
| All BOR and PVD thresholds excepting BOR0 | - | 100 | - |

1. Guaranteed by characterization results.

2. Valid for device version without BOR at power up. Please see option "D" in Ordering information scheme for more details.

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**STM32L031x4/6 Electrical characteristics**

**6.3.3 Embedded internal reference voltage**

The parameters given in *Table 23* are based on characterization results, unless otherwise specified.

**Table 22. Embedded internal reference voltage calibration values**

| **Calibration value name** | **Description** | **Memory address** |
| --- | --- | --- |
| VREFINT\_CAL | Raw data acquired at temperature of 25 °C, VDDA= 3 V | 0x1FF8 0078 - 0x1FF8 0079 |

**Table 23. Embedded internal reference voltage(1)**

| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| --- | --- | --- | --- | --- | --- | --- |
| VREFINT out(2) | Internal reference voltage | – 40 °C < TJ < +125 °C | 1.202 | 1.224 | 1.242 | V |
| TVREFINT | Internal reference startup time | - | - | 2 | 3 | ms |
| VVREF\_MEAS | VDDA voltage during VREFINT factory measure | - | 2.99 | 3 | 3.01 | V |
| AVREF\_MEAS | Accuracy of factory-measured VREFINT value(3) | Including uncertainties due to ADC and VDDA values | - | - | ±5 | mV |
| TCoeff(4) | Temperature coefficient | –40 °C < TJ < +125 °C | - | 25 | 100 | ppm/°C |
| ACoeff(4) | Long-term stability | 1000 hours, T = 25 °C | - | - | 1000 | ppm |
| VDDCoeff(4) | Voltage coefficient | 3.0 V < VDDA < 3.6 V | - | - | 2000 | ppm/V |
| TS\_vrefint(4)(5) | ADC sampling time when reading the internal reference voltage | - | 5 | 10 | - | µs |
| TADC\_BUF(4) | Startup time of reference voltage buffer for ADC | - | - | - | 10 | µs |
| IBUF\_ADC(4) | Consumption of reference voltage buffer for ADC | - | - | 13.5 | 25 | µA |
| IVREF\_OUT(4) | VREF\_OUT output current(6) | - | - | - | 1 | µA |
| CVREF\_OUT(4) | VREF\_OUT output load | - | - | - | 50 | pF |
| ILPBUF(4) | Consumption of reference voltage buffer for VREF\_OUT and COMP | - | - | 730 | 1200 | nA |
| VREFINT\_DIV1(4) | 1/4 reference voltage | - | 24 | 25 | 26 | %  VREFINT |
| VREFINT\_DIV2(4) | 1/2 reference voltage | - | 49 | 50 | 51 |
| VREFINT\_DIV3(4) | 3/4 reference voltage | - | 74 | 75 | 76 |

1. Refer to *Table 35: Peripheral current consumption in Stop and Standby mode* for the value of the internal reference current consumption (IREFINT).

2. Guaranteed by test in production.

3. The internal VREF value is individually measured in production and stored in dedicated EEPROM bytes. 4. Guaranteed by design.

5. Shortest sampling time can be determined in the application by multiple iterations.

6. To guarantee less than 1% VREF\_OUT deviation.

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**Electrical characteristics STM32L031x4/6**

**6.3.4 Supply current characteristics**

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in *Figure 14: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code if not specified otherwise.

The current consumption values are derived from the tests performed under ambient temperature and VDD supply voltage conditions summarized in *Table 20: General operating conditions* unless otherwise specified.

The MCU is placed under the following conditions:

• All I/O pins are configured in analog input mode

• All peripherals are disabled except when explicitly mentioned

• The Flash memory access time and prefetch is adjusted depending on fHCLK frequency and voltage range to provide the best CPU performance unless otherwise specified.

• When the peripherals are enabled fAPB1 = fAPB2 = fAPB

• When PLL is on, the PLL inputs are equal to HSI = 16 MHz (if internal clock is used) or HSE = 16 MHz (if HSE bypass mode is used)

• The HSE user clock is applied to OSCI\_IN input (LQFP48 package) and to CK\_IN (other packages). It follows the characteristic specified in *Table 37: High-speed external user clock characteristics*

• For maximum current consumption VDD = VDDA = 3.6 V is applied to all supply pins • For typical current consumption VDD = VDDA = 3.0 V is applied to all supply pins if not specified otherwise

The parameters given in *Table 44*, *Table 20* and *Table 21* are derived from tests performed under ambient temperature and VDD supply voltage conditions summarized in *Table 20*.

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**STM32L031x4/6 Electrical characteristics**

**Table 24. Current consumption in Run mode, code with data processing running from Flash memory**

| **Symbol** | **Parameter** | **Conditions** | | **fHCLK** | **Typ** | **Max(1)** | **Unit** |
| --- | --- | --- | --- | --- | --- | --- | --- |
| IDD  (Run  from  Flash) | Supply  current in  Run mode,  code  executed  from Flash | fHSE = fHCLK up to 16 MHz included, fHSE = fHCLK/2 above 16 MHz (PLL on)(2) | Range 3, VCORE = 1.2 V VOS[1:0] = 11 | 1 MHz | 140 | 200 | µA |
| 2 MHz | 245 | 310 |
| 4 MHz | 460 | 540 |
| Range 2, VCORE = 1.5 V, VOS[1:0] = 10, | 4 MHz | 0.56 | 0.63 | mA |
| 8 MHz | 1.1 | 1.2 |
| 16 MHz | 2.1 | 2.3 |
| Range 1, VCORE = 1.8 V, VOS[1:0] = 01 | 8 MHz | 1.25 | 1.4 |
| 16 MHz | 2.5 | 2.7 |
| 32 MHz | 5 | 5.6 |
| HSI clock | Range 2, VCORE = 1.5 V, VOS[1:0] = 10, | 16 MHz | 2.1 | 2.4 |
| Range 1, VCORE = 1.8 V, VOS[1:0] = 01 | 32 MHz | 5.1 | 5.7 |
| MSI clock | Range 3, VCORE = 1.2 V, VOS[1:0] = 11 | 65 kHz | 34.5 | 110 | µA |
| 524 kHz | 86 | 150 |
| 4.2 MHz | 505 | 570 |

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

2. Oscillator bypassed (HSEBYP = 1 in RCC\_CR register).

**Table 25. Current consumption in Run mode vs code type,**

**code with data processing running from Flash memory**

| **Symbol** | **Parameter** | **Conditions** | | | **fHCLK** | **Typ** | **Unit** |
| --- | --- | --- | --- | --- | --- | --- | --- |
| IDD  (Run  from  Flash) | Supply  current in  Run mode,  code  executed  from Flash  memory | fHSE = fHCLK up to 16 MHz included, fHSE = fHCLK/2 above 16 MHz (PLL ON)(1) | Range 3,  VCORE=1.2 V, VOS[1:0] = 11 | Dhrystone | 4 MHz | 460 | µA |
| CoreMark | 455 |
| Fibonacci | 330 |
| while(1) | 305 |
| while(1), prefetch OFF | 320 |
| Range 1,  VOS[1:0] = 01, VCORE = 1.8 V | Dhrystone | 32 MHz | 5 | mA |
| CoreMark | 5.15 |
| Fibonacci | 5 |
| while(1) | 4.35 |
| while(1), prefetch OFF | 3.85 |

1. Oscillator bypassed (HSEBYP = 1 in RCC\_CR register).

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**Electrical characteristics STM32L031x4/6**

**Figure 15. IDD vs VDD, at TA= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSE = 16 MHz, 1WS**

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| --- |

**Figure 16. IDD vs VDD, at TA= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSI16, 1WS**

| ,''  (  (  (  (  (    ~~9~~''    ŚƌǇƐƚŽŶĞ Ϯ͘ϭͲ ϭ t^͕ ʹ ϰϬΣ  ŚƌǇƐƚŽŶĞ Ϯ͘ϭͲ ϭ t^͕ ϮϱΣ  ŚƌǇƐƚŽŶĞ Ϯ͘ϭ Ͳ ϭ t^͕ ϱϱΣ  ŚƌǇƐƚŽŶĞ Ϯ͘ϭͲ ϭ t^͕ ϴϱΣ  ŚƌǇƐƚŽŶĞ Ϯ͘ϭͲ ϭ t^͕ ϭϬϱΣ  ŚƌǇƐƚŽŶĞ Ϯ͘ϭͲ ϭ t^͕ ϭϮϱΣ  06Y 9 |
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**Table 26. Current consumption in Run mode, code with data processing running from RAM**

| **Symbol** | **Parameter** | **Conditions** | | **fHCLK** | **Typ** | **Max(1)** | **Unit** |
| --- | --- | --- | --- | --- | --- | --- | --- |
| IDD (Run from  RAM) | Supply current in Run mode, code executed from RAM, Flash  switched OFF | fHSE = fHCLK up to 16 MHz, included  fHSE = fHCLK/2 above 16 MHz  (PLL ON)(2) | Range 3,  VCORE = 1.2 V,  VOS[1:0] = 11 | 1 MHz | 115 | 170 | µA |
| 2 MHz | 210 | 250 |
| 4 MHz | 385 | 420 |
| Range 2,  VCORE = 1.5 ,V,  VOS[1:0] = 10 | 4 MHz | 0.48 | 0.6 | mA |
| 8 MHz | 0.935 | 1.1 |
| 16 MHz | 1.8 | 2 |
| Range 1,  VCORE = 1.8 V,  VOS[1:0] = 01 | 8 MHz | 1.1 | 1.3 |
| 16 MHz | 2.1 | 2.3 |
| 32 MHz | 4.5 | 4.7 |
| MSI clock | Range 3,  VCORE = 1.2 V,  VOS[1:0] = 11 | 65 kHz | 22 | 52 | µA |
| 524 kHz | 70.5 | 91 |
| 4.2 MHz | 420 | 450 |
| HSI16 clock source (16 MHz) | Range 2,  VCORE = 1.5 V,  VOS[1:0] = 10 | 16 MHz | 1.95 | 2.2 | mA |
| Range 1,  VCORE = 1.8 V,  VOS[1:0] = 01 | 32 MHz | 4.7 | 5.1 |

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

2. Oscillator bypassed (HSEBYP = 1 in RCC\_CR register).

**Table 27. Current consumption in Run mode vs code type,**

**code with data processing running from RAM(1)**

| **Symbol** | **Parameter** | **Conditions** | | | **fHCLK** | **Typ** | **Unit** |
| --- | --- | --- | --- | --- | --- | --- | --- |
| IDD (Run from  RAM) | Supply current in Run mode, code executed from RAM, Flash  switched OFF | fHSE = fHCLK up to 16 MHz, included,  fHSE = fHCLK/2 above 16 MHz (PLL ON)(2) | Range 3,  VCORE = 1.2 V,  VOS[1:0] = 11 | Dhrystone | 4 MHz | 385 | µA |
| CoreMark | 395 |
| Fibonacci | 360 |
| while(1) | 265 |
| Range 1,  VCORE = 1.8 V,  VOS[1:0] = 01 | Dhrystone | 32 MHz | 4.5 | mA |
| CoreMark | 4.65 |
| Fibonacci | 4.2 |
| while(1) | 3.05 |

1. Guaranteed by characterization results, unless otherwise specified.

2. Oscillator bypassed (HSEBYP = 1 in RCC\_CR register).

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**Table 28. Current consumption in Sleep mode**

| **Symbol** | **Parameter** | **Conditions** | | **fHCLK** | **Typ** | **Max(1)** | **Unit** |
| --- | --- | --- | --- | --- | --- | --- | --- |
| IDD (Sleep) | Supply current in Sleep  mode, Flash memory OFF | fHSE = fHCLK up to 16 MHz included, fHSE = fHCLK/2  above 16 MHz (PLL ON)(2) | Range 3,  VCORE = 1.2 V,  VOS[1:0] = 11 | 1 MHz | 36.5 | 87 | µA |
| 2 MHz | 58 | 100 |
| 4 MHz | 100 | 170 |
| Range 2,  VCORE = 1.5 V,  VOS[1:0] = 10 | 4 MHz | 125 | 190 |
| 8 MHz | 230 | 310 |
| 16 MHz | 450 | 540 |
| Range 1,  VCORE = 1.8 V,  VOS[1:0] = 01 | 8 MHz | 275 | 360 |
| 16 MHz | 555 | 650 |
| 32 MHz | 1350 | 1600 |
| HSI16 clock source (16 MHz) | Range 2,  VCORE = 1.5 V,  VOS[1:0] = 10 | 16 MHz | 585 | 690 |
| Range 1,  VCORE = 1.8 V,  VOS[1:0] = 01 | 32 MHz | 1500 | 1700 |
| MSI clock | Range 3,  VCORE = 1.2 V,  VOS[1:0] = 11 | 65 kHz | 17 | 43 |
| 524 kHz | 28 | 55 |
| 4.2 MHz | 115 | 190 |
| Supply current in Sleep  mode, Flash memory ON | fHSE = fHCLK up to 16 MHz included, fHSE = fHCLK/2  above 16 MHz (PLL ON)(2) | Range 3,  VCORE =1.2 V,  VOS[1:0] = 11 | 1 MHz | 49 | 160 |
| 2 MHz | 69 | 190 |
| 4 MHz | 115 | 230 |
| Range 2,  VCORE = 1.5 V,  VOS[1:0] = 10 | 4 MHz | 135 | 200 |
| 8 MHz | 240 | 320 |
| 16 MHz | 460 | 550 |
| Range 1,  VCORE = 1.8 V,  VOS[1:0]=01 | 8 MHz | 290 | 370 |
| 16 MHz | 565 | 670 |
| 32 MHz | 1350 | 1600 |
| HSI16 clock source (16 MHz) | Range 2,  VCORE = 1.5 V,  VOS[1:0]=10 | 16 MHz | 600 | 700 |
| Range 1,  VCORE = 1.8 V,  VOS[1:0] = 01 | 32 MHz | 1500 | 1700 |
| MSI clock | Range 3,  VCORE = 1.2 V,  VOS[1:0] = 11 | 65 kHz | 28 | 55 |
| 524 kHz | 39.5 | 67 |
| 4.2 MHz | 125 | 200 |

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

2. Oscillator bypassed (HSEBYP = 1 in RCC\_CR register).

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**Table 29. Current consumption in Low-power run mode**

| **Symbol** | **Parameter** | **Conditions** | | | **Typ** | **Max(1)** | **Unit** |
| --- | --- | --- | --- | --- | --- | --- | --- |
| IDD  (LP Run) | Supply  current in  Low-power run mode | All  peripherals off, code  executed  from RAM, Flash  memory  OFF, VDD  from 1.65 V to 3.6 V | MSI clock, 65 kHz fHCLK = 32 kHz | TA = -40 °C to 25 °C | 6.3 | 8.4 | µA |
| TA = 85 °C | 9.15 | 13 |
| TA = 105 °C | 12.5 | 19 |
| TA = 125 °C | 20.5 | 36 |
| MSI clock, 65 kHz fHCLK = 65 kHz | TA =-40 °C to 25 °C | 9.45 | 12 |
| TA = 85 °C | 12.5 | 15 |
| TA = 105 °C | 16 | 22 |
| TA = 125 °C | 24 | 38 |
| MSI clock, 131 kHz fHCLK = 131 kHz | TA = -40 °C to 25 °C | 17 | 20 |
| TA = 55 °C | 19 | 21 |
| TA = 85 °C | 20.5 | 24 |
| TA = 105 °C | 23.5 | 28 |
| TA = 125 °C | 31.5 | 46 |
| All  peripherals off, code  executed  from Flash memory,  VDD from  1.65 V to  3.6 V | MSI clock, 65 kHz fHCLK = 32 kHz | TA = -40 °C to 25 °C | 18.5 | 23 |
| TA = 85 °C | 23 | 27 |
| TA = 105 °C | 27 | 33 |
| TA = 125 °C | 36 | 52 |
| MSI clock, 65 kHz fHCLK = 65 kHz | TA = -40 °C to 25 °C | 22.5 | 26 |
| TA = 85 °C | 27.5 | 31 |
| TA = 105 °C | 31 | 38 |
| TA = 125 °C | 40.5 | 56 |
| MSI clock, 131 kHz fHCLK = 131 kHz | TA = -40 °C to 25 °C | 32 | 36 |
| TA = 55 °C | 35 | 37 |
| TA = 85 °C | 37.5 | 42 |
| TA = 105 °C | 41 | 47 |
| TA = 125 °C | 50 | 65 |

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

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**Figure 17. IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS**

| ,''  (  (  (  (  (  (    9''  &  &  &  &  &  &  06Y 9 |
| --- |

**Table 30. Current consumption in Low-power sleep mode**

| **Symbol** | **Parameter** | **Conditions** | | | **Typ** | **Max(1)** | **Unit** |
| --- | --- | --- | --- | --- | --- | --- | --- |
| IDD  (LP Sleep) | Supply  current in Low-power sleep mode | All peripherals off, VDD from  1.65 V to 3.6 V | MSI clock, 65 kHz fHCLK = 32 kHz  Flash memory OFF | TA = -40 °C to 25 °C | 3.2(2) | - | µA |
| MSI clock, 65 kHz fHCLK = 32 kHz  Flash memory ON | TA = -40 °C to 25 °C | 13 | 19 |
| TA = 85 °C | 16 | 21 |
| TA = 105 °C | 18.5 | 24 |
| TA = 125 °C | 23.5 | 32 |
| MSI clock, 65 kHz fHCLK = 65 kHz, Flash memory ON | TA = -40 °C to 25 °C | 13.5 | 19 |
| TA = 85 °C | 16.5 | 21 |
| TA = 105 °C | 18.5 | 24 |
| TA = 125 °C | 24 | 33 |
| MSI clock, 131 kHz fHCLK = 131 kHz, Flash memory ON | TA = -40 °C to 25 °C | 15.5 | 21 |
| TA = 55 °C | 17.5 | 22 |
| TA = 85 °C | 18.5 | 23 |
| TA = 105 °C | 21 | 26 |
| TA = 125 °C | 26 | 35 |

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

2. As the CPU is in Sleep mode, the difference between the current consumption with Flash memory ON and OFF (nearly 12 µA) is the same whatever the clock frequency.

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**Table 31. Typical and maximum current consumptions in Stop mode**

| **Symbol** | **Parameter** | **Conditions** | **Typ** | **Max(1)** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| IDD (Stop) | Supply current in Stop mode | TA = -40°C to 25°C | 0.38 | 0.99 | µA |
| TA = 55°C | 0.54 | 1.9 |
| TA= 85°C | 1.35 | 4.2 |
| TA = 105°C | 3.1 | 9 |
| TA = 125°C | 7.55 | 19 |

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

**Figure 18. IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive**

| (  (  (  (  (  (  (  (  (  (    &  &  &  &  &  &  06Y 9 |
| --- |

**Figure 19. IDD vs VDD, at TA= 25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks off**

| ,''  (  (  (  (  (  (  (  (  (    9''    &  &  &  &  &  &  06Y 9 |
| --- |

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**Table 32. Typical and maximum current consumptions in Standby mode**

| **Symbol** | **Parameter** | **Conditions** |  | **Typ** | **Max(1)** | **Unit** |
| --- | --- | --- | --- | --- | --- | --- |
| IDD  (Standby) | Supply current in Standby mode | Independent watchdog and LSI enabled | TA = -40 °C to 25 °C | 0.8 | 1.6 | µA |
| TA = 55 °C | 0.9 | 1.8 |
| TA= 85 °C | 1 | 2 |
| TA = 105 °C | 1.3 | 3 |
| TA = 125 °C | 2.15 | 7 |
| Independent watchdog and LSI off | TA = -40 °C to 25 °C | 0.255 | 0.6 |
| TA = 55 °C | 0.28 | 0.7 |
| TA = 85 °C | 0.405 | 1 |
| TA = 105 °C | 0.7 | 1.7 |
| TA = 125 °C | 1.55 | 5 |

1. Guaranteed by characterization results at 125 °C, unless otherwise specified

**Table 33. Average current consumption during wakeup**

| **Symbol** | **parameter** | **System frequency** | **Current**  **consumption**  **during wakeup** | **Unit** |
| --- | --- | --- | --- | --- |
| IDD (WU from  Stop) | Supply current during wakeup from Stop mode | HSI | 1 | mA |
| HSI/4 | 0.7 |
| MSI 4,2 MHz | 0.7 |
| MSI 1,05 MHz | 0.4 |
| MSI 65 KHz | 0.1 |
| IDD (Reset) | Reset pin pulled down | - | 0.21 |
| IDD (Power Up) | BOR on | - | 0.23 |
| IDD (WU from  StandBy) | With Fast wakeup set | MSI 2,1 MHz | 0.5 |
| With Fast wakeup disabled | MSI 2,1 MHz | 0.12 |

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**On-chip peripheral current consumption**

The current consumption of the on-chip peripherals is given in the following tables. The MCU is placed under the following conditions:

• all I/O pins are in input mode with a static value at VDD or VSS (no load)

• all peripherals are disabled unless otherwise mentioned

• the given value is calculated by measuring the current consumption

– with all peripherals clocked off

– with only one peripheral clocked on

**Table 34. Peripheral current consumption in Run or Sleep mode(1)**

| **Peripheral** | | **Typical consumption, VDD = 3.0 V, TA = 25 °C** | | | | **Unit** |
| --- | --- | --- | --- | --- | --- | --- |
| **Range 1,**  **VCORE=1.8 V VOS[1:0] = 01** | **Range 2,**  **VCORE=1.5 V VOS[1:0] = 10** | **Range 3,**  **VCORE=1.2 V VOS[1:0] = 11** | **Low-power**  **sleep and run** |
| APB1 | WWDG | 3 | 2 | 2 | 2 | µA/MHz (fHCLK) |
| LPUART1 | 8 | 6.5 | 5.5 | 6 |
| I2C1 | 11 | 9.5 | 7.5 | 9 |
| LPTIM1 | 10 | 8.5 | 6.5 | 8 |
| TIM2 | 10.5 | 8.5 | 7 | 9 |
| USART2 | 14.5 | 12 | 9.5 | 11 |
| APB2 | ADC1(2) | 5.5 | 5 | 3.5 | 4 | µA/MHz (fHCLK) |
| SPI1 | 4 | 3 | 3 | 2.5 |
| TIM21 | 7.5 | 6 | 5 | 5.5 |
| TIM22 | 7 | 6 | 5 | 6 |
| DBGMCU | 1.5 | 1 | 1 | 0.5 |
| SYSCFG | 2.5 | 2 | 2 | 1.5 |
| Cortex  M0+ core I/O port | GPIOA | 3.5 | 3 | 2.5 | 2.5 | µA/MHz (fHCLK) |
| GPIOB | 3.5 | 2.5 | 2 | 2.5 |
| GPIOC | 8.5 | 6.5 | 5.5 | 7 |
| GPIOH | 1.5 | 1 | 1 | 0.5 |
| AHB | CRC | 1.5 | 1 | 1 | 1 | µA/MHz (fHCLK) |
| FLASH | 0(3) | 0(3) | 0(3) | 0(3) |
| DMA1 | 10 | 8 | 6.5 | 8.5 |
| All enabled | | 101 | 83 | 66 | 85 |
| PWR | | 2.5 | 2 | 2 | 1 | µA/MHz (fHCLK) |

1. Data based on differential IDD measurement between all peripherals off an one peripheral with clock enabled, in the following conditions: fHCLK = 32 MHz (range 1), fHCLK = 16 MHz (range 2), fHCLK = 4 MHz (range 3), fHCLK = 64kHz (Low-power run/sleep), fAPB1 = fHCLK, fAPB2 = fHCLK, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling. Not tested in production.

2. HSI oscillator is off for this measure.

3. Current consumption is negligible and close to 0 µA.

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**Table 35. Peripheral current consumption in Stop and Standby mode(1)**

| **Symbol** | **Peripheral** | **Typical consumption, TA = 25 °C** | | **Unit** |
| --- | --- | --- | --- | --- |
| **VDD=1.8 V** | **VDD=3.0 V** |
| IDD(PVD / BOR) | - | 0.7 | 1.2 | µA |
| IREFINT | - | 1.3 | 1.4 |
| - | LSE Low drive(2) | 0.1 | 0.1 |
| - | LSI | 0.27 | 0.31 |
| - | IWDG | 0.2 | 0.3 |
| - | LPTIM1, Input 100 Hz | 0.01 | 0.01 |
| - | LPTIM1, Input 1 MHz | 6 | 6 |
| - | LPUART1 | 0.2 | 0.2 |
| - | RTC (LSE in Bypass mode) | 0.2 | 0.2 |

1. LPTIM, LPUART peripherals can operate in Stop mode but not in Standby mode

2. LSE Low drive consumption is the difference between an external clock on OSC32\_IN and a quartz between OSC32\_IN and OSC32\_OUT.

**6.3.5 Wakeup time from low-power mode**

The wakeup times given in the following table are measured with the MSI or HSI16 RC oscillator. The clock source used to wake up the device depends on the current operating mode:

• Sleep mode: the clock source is the clock that was set before entering Sleep mode • Stop mode: the clock source is either the MSI oscillator in the range configured before entering Stop mode, the HSI16 or HSI16/4.

• Standby mode: the clock source is the MSI oscillator running at 2.1 MHz

All timings are derived from tests performed under ambient temperature and VDD supply voltage conditions summarized in *Table 20*.

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**Table 36. Low-power mode wakeup timings**

| **Symbol** | **Parameter** | **Conditions** | **Typ** | **Max** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| tWUSLEEP | Wakeup from Sleep mode | fHCLK = 32 MHz | 7 | 8 | Number of clock cycles |
| tWUSLEEP\_ LP | Wakeup from Low-power sleep mode, fHCLK = 262 kHz | fHCLK = 262 kHz  Flash memory enabled | 7 | 8 |
| fHCLK = 262 kHz  Flash memory switched OFF | 9 | 10 |
| tWUSTOP | Wakeup from Stop mode, regulator in Run mode | fHCLK = fMSI = 4.2 MHz | 5.0 | 8 | µs |
| fHCLK = fHSI = 16 MHz | 4.9 | 7 |
| fHCLK = fHSI/4 = 4 MHz | 8.0 | 11 |
| Wakeup from Stop mode, regulator in low power mode | fHCLK = fMSI = 4.2 MHz Voltage range 1 | 5.0 | 8 |
| fHCLK = fMSI = 4.2 MHz Voltage range 2 | 5.0 | 8 |
| fHCLK = fMSI = 4.2 MHz Voltage range 3 | 5.0 | 8 |
| fHCLK = fMSI = 2.1 MHz | 7.3 | 13 |
| fHCLK = fMSI = 1.05 MHz | 13 | 23 |
| fHCLK = fMSI = 524 kHz | 28 | 38 |
| fHCLK = fMSI = 262 kHz | 51 | 65 |
| fHCLK = fMSI = 131 kHz | 100 | 120 |
| fHCLK = MSI = 65 kHz | 200 | 260 |
| fHCLK = fHSI = 16 MHz | 4.9 | 7 |
| fHCLK = fHSI/4 = 4 MHz | 8.0 | 11 |
| Wakeup from Stop mode, regulator in low power mode, code running from RAM | fHCLK = fHSI = 16 MHz | 4.9 | 7 |
| fHCLK = fHSI/4 = 4 MHz | 7.9 | 10 |
| fHCLK = fMSI = 4.2 MHz | 4.7 | 8 |
| tWUSTDBY | Wakeup from Standby mode  FWU bit = 1 | fHCLK = MSI = 2.1 MHz | 65 | 130 |
| Wakeup from Standby mode  FWU bit = 0 | fHCLK = MSI = 2.1 MHz | 2.2 | 3 | ms |

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**Electrical characteristics STM32L031x4/6**

**6.3.6 External clock source characteristics**

**High-speed external user clock generated from an external source**

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.The external clock signal has to respect the I/O characteristics in *Section 6.3.12*. However, the recommended clock input waveform is shown in *Figure 20*.

**Table 37. High-speed external user clock characteristics(1)**

| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| --- | --- | --- | --- | --- | --- | --- |
| fHSE\_ext | User external clock source  frequency | CSS is on or PLL is used | 1 | 8 | 32 | MHz |
| CSS is off, PLL not used | 0 | 8 | 32 | MHz |
| VHSEH | OSC\_IN/CK\_IN(2) input pin high level voltage | - | 0.7VDD | - | VDD | V |
| VHSEL | OSC\_IN/CK\_IN(2) input pin low level voltage | VSS | - | 0.3VDD |
| tw(HSE)  tw(HSE) | OSC\_IN/CK\_IN(2) high or low time | 12 | - | - | ns |
| tr(HSE)  tf(HSE) | OSC\_IN/CK\_IN(2) rise or fall time | - | - | 20 |
| Cin(HSE) | OSC\_IN/CK\_IN(2) input capacitance | - | 2.6 | - | pF |
| DuCy(HSE) | Duty cycle | 45 | - | 55 | % |
| IL | OSC\_IN/CK\_IN(2) Input leakage current | VSS ≤ VIN ≤ VDD | - | - | ±1 | µA |

1. Guaranteed by design.

2. HSE external user clock is applied to OSC\_IN on LQFP48 package and to CK\_IN on other packages.

**Figure 20. High-speed external clock source AC timing diagram**

| 9+6(+      9+6(/  W WU +6( W: +6(  WI +6( W: +6(  ~~7~~+6(  I+6(BH[W  (;7(51$/  ,/  26&B,1  &/2&. 6285&(  670 /[[  DL F |
| --- |

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**STM32L031x4/6 Electrical characteristics**

**Low-speed external user clock generated from an external source**

The characteristics given in the following table result from tests performed using a low speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 20*.

**Table 38. Low-speed external user clock characteristics(1)**

| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| --- | --- | --- | --- | --- | --- | --- |
| fLSE\_ext | User external clock source frequency | - | 1 | 32.768 | 1000 | kHz |
| VLSEH | OSC32\_IN input pin high level voltage | 0.7VDD | - | VDD | V |
| VLSEL | OSC32\_IN input pin low level voltage | VSS | - | 0.3VDD |
| tw(LSE)  tw(LSE) | OSC32\_IN high or low time | 465 | - | - | ns |
| tr(LSE)  tf(LSE) | OSC32\_IN rise or fall time | - | - | 10 |
| CIN(LSE) | OSC32\_IN input capacitance | - | - | 0.6 | - | pF |
| DuCy(LSE) | Duty cycle | - | 45 | - | 55 | % |
| IL | OSC32\_IN Input leakage current | VSS ≤ VIN ≤ VDD | - | - | ±1 | µA |

1. Guaranteed by design.

**Figure 21. Low-speed external clock source AC timing diagram**

| 9/6(+      9/6(/  W WU /6( W: /6(  WI /6( W: /6(  ~~7~~/6(  I/6(BH[W  26& B,1 (;7(51$/  ,/  &/2&. 6285&(  670 /[[  DL F |
| --- |

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**Electrical characteristics STM32L031x4/6**

**High-speed external clock generated from a crystal/ceramic resonator**

The high-speed external (HSE) clock can be supplied with a 1 to 25 MHz crystal/ceramic resonator oscillator (LQFP48 package only). All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 39*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 39. HSE oscillator characteristics(1)**

| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| --- | --- | --- | --- | --- | --- | --- |
| fOSC\_IN | Oscillator frequency | - | 1 |  | 25 | MHz |
| RF | Feedback resistor | - | - | 200 | - | kΩ |
| Gm | Maximum critical crystal  transconductance | Startup | - | - | 700 | µA  /V |
| tSU(HSE) (2) | Startup time | VDD is stabilized | - | 2 | - | ms |

1. Guaranteed by design.

2. Guaranteed by characterization results. tSU(HSE) is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For CL1 and CL2, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 22*). CL1 and CL2 are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of CL1 and CL2. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing CL1 and CL2. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

**Figure 22. HSE oscillator circuit diagram**

| I+6( WR FRUH  5P  5)  /P&2  &/  26&B,1  &P  JP  5HVRQDWRU  &RQVXPSWLRQ  FRQWURO  5HVRQDWRU  670  26&B287  &/  DL E |
| --- |

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**STM32L031x4/6 Electrical characteristics**

**Low-speed external clock generated from a crystal/ceramic resonator**

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 40*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 40. LSE oscillator characteristics(1)**

| **Symbol** | **Parameter** | **Conditions(2)** | **Min(2)** | **Typ** | **Max** | **Unit** |
| --- | --- | --- | --- | --- | --- | --- |
| fLSE | LSE oscillator frequency |  | - | 32.768 | - | kHz |
| Gm | Maximum critical crystal transconductance | LSEDRV[1:0]=00  lower driving capability | - | - | 0.5 | µA/V |
| LSEDRV[1:0]= 01  medium low driving capability | - | - | 0.75 |
| LSEDRV[1:0] = 10  medium high driving capability | - | - | 1.7 |
| LSEDRV[1:0]=11  higher driving capability | - | - | 2.7 |
| tSU(LSE)(3) | Startup time | VDD is stabilized | - | 2 | - | s |

1. Guaranteed by design.

2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.

3. Guaranteed by characterization results. tSU(LSE) is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer. To increase speed, address a lower-drive quartz with a high- driver mode.

*Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.*

**Figure 23. Typical application with a 32.768 kHz crystal**

| 5HVRQDWRU ZLWK LQWHJUDWHG  FDSDFLWRUV  &/  26& B,1  I/6(  'ULYH  N+]  SURJUDPPDEOH  UHVRQDWRU  DPSOLILHU  26& B287  &/  06 9 |
| --- |

*Note: An external resistor is not required between OSC32\_IN and OSC32\_OUT and it is forbidden to add one.*

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**6.3.7 Internal clock source characteristics**

The parameters given in *Table 41* are derived from tests performed under ambient temperature and VDD supply voltage conditions summarized in *Table 20*.

**High-speed internal 16 MHz (HSI16) RC oscillator**

**Table 41. 16 MHz HSI16 oscillator characteristics**

| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| --- | --- | --- | --- | --- | --- | --- |
| fHSI16 | Frequency | VDD = 3.0 V | - | 16 | - | MHz |
| TRIM(1)(2) | HSI16 user  trimmed resolution | Trimming code is not a multiple of 16 | - | ± 0.4 | 0.7 | % |
| Trimming code is a multiple of 16 | - | - | ± 1.5 | % |
| ACCHSI16 (2) | Accuracy of the factory-calibrated HSI16 oscillator | VDDA = 3.0 V, TA = 25 °C | –1(3) | - | 1(3) | % |
| VDDA = 3.0 V, TA = 0 to 55 °C | –1.5 | - | 1.5 | % |
| VDDA = 3.0 V, TA = -10 to 70 °C | –2 | - | 2 | % |
| VDDA = 3.0 V, TA = -10 to 85 °C | –2.5 | - | 2 | % |
| VDDA = 3.0 V, TA = -10 to 105 °C | –4 | - | 2 | % |
| VDDA = 1.65 V to 3.6 V  TA = -40 to 125 °C | –5.45 | - | 3.25 | % |
| tSU(HSI16)(2) | HSI16 oscillator startup time | - | - | 3.7 | 6 | µs |
| IDD(HSI16)(2) | HSI16 oscillator power consumption | - | - | 100 | 140 | µA |

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).

2. Guaranteed by characterization results.

3. Guaranteed by test in production.

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**Figure 24. HSI16 minimum and maximum value versus temperature**

| 9 PLQ    9 W\S    9 PD[    9 PD[    9 PLQ          06Y 9 |
| --- |

**Low-speed internal (LSI) RC oscillator**

**Table 42. LSI oscillator characteristics**

| **Symbol** | **Parameter** | **Min** | **Typ** | **Max** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| fLSI(1) | LSI frequency | 26 | 38 | 56 | kHz |
| DLSI(2) | LSI oscillator frequency drift  0°C ≤ TA ≤ 85°C | –10 | - | 4 | % |
| tsu(LSI)(3) | LSI oscillator startup time | - | - | 200 | µs |
| IDD(LSI)(3) | LSI oscillator power consumption | - | 400 | 510 | nA |

1. Guaranteed by test in production.

2. This is a deviation for an individual part, once the initial frequency has been measured. 3. Guaranteed by design.

**Multi-speed internal (MSI) RC oscillator**

**Table 43. MSI oscillator characteristics**

| **Symbol** | **Parameter** | **Condition** | **Typ** | **Max** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| fMSI | Frequency after factory calibration, done at VDD= 3.3 V and TA = 25 °C | MSI range 0 | 65.5 | - | kHz |
| MSI range 1 | 131 | - |
| MSI range 2 | 262 | - |
| MSI range 3 | 524 | - |
| MSI range 4 | 1.05 | - | MHz |
| MSI range 5 | 2.1 | - |
| MSI range 6 | 4.2 | - |
| ACCMSI | Frequency error after factory calibration | - | ±0.5 | - | % |

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**Table 43. MSI oscillator characteristics (continued)**

| **Symbol** | **Parameter** | **Condition** | **Typ** | **Max** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| DTEMP(MSI)(1) | MSI oscillator frequency drift  0 °C ≤ TA ≤ 85 °C | - | ±3 | - | % |
| DVOLT(MSI)(1) | MSI oscillator frequency drift  1.65 V ≤ VDD ≤ 3.6 V, TA = 25 °C | - | - | 2.5 | %/V |
| IDD(MSI)(2) | MSI oscillator power consumption | MSI range 0 | 0.75 | - | µA |
| MSI range 1 | 1 | - |
| MSI range 2 | 1.5 | - |
| MSI range 3 | 2.5 | - |
| MSI range 4 | 4.5 | - |
| MSI range 5 | 8 | - |
| MSI range 6 | 15 | - |
| tSU(MSI) | MSI oscillator startup time | MSI range 0 | 30 | - | µs |
| MSI range 1 | 20 | - |
| MSI range 2 | 15 | - |
| MSI range 3 | 10 | - |
| MSI range 4 | 6 | - |
| MSI range 5 | 5 | - |
| MSI range 6, Voltage range 1 and 2 | 3.5 | - |
| MSI range 6, Voltage range 3 | 5 | - |
| tSTAB(MSI)(2) | MSI oscillator stabilization time | MSI range 0 | - | 40 | µs |
| MSI range 1 | - | 20 |
| MSI range 2 | - | 10 |
| MSI range 3 | - | 4 |
| MSI range 4 | - | 2.5 |
| MSI range 5 | - | 2 |
| MSI range 6, Voltage range 1 and 2 | - | 2 |
| MSI range 3, Voltage range 3 | - | 3 |
| fOVER(MSI) | MSI oscillator frequency overshoot | Any range to range 5 | - | 4 | MHz |
| Any range to range 6 | - | 6 |

1. This is a deviation for an individual part, once the initial frequency has been measured. 2. Guaranteed by characterization results.

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**6.3.8 PLL characteristics**

The parameters given in *Table 44* are derived from tests performed under ambient temperature and VDD supply voltage conditions summarized in *Table 20*.

**Table 44. PLL characteristics**

| **Symbol** | **Parameter** | **Value** | | | **Unit** |
| --- | --- | --- | --- | --- | --- |
| **Min** | **Typ** | **Max(1)** |
| fPLL\_IN | PLL input clock(2) | 2 | - | 24 | MHz |
| PLL input clock duty cycle | 45 | - | 55 | % |
| fPLL\_OUT | PLL output clock | 2 | - | 32 | MHz |
| tLOCK | PLL input = 16 MHz  PLL VCO = 96 MHz | - | 115 | 160 | µs |
| Jitter | Cycle-to-cycle jitter | - |  | ± 600 | ps |
| IDDA(PLL) | Current consumption on VDDA | - | 220 | 450 | µA |
| IDD(PLL) | Current consumption on VDD | - | 120 | 150 |

1. Guaranteed by characterization results.

2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by fPLL\_OUT.

**6.3.9 Memory characteristics**

**RAM memory**

**Table 45. RAM and hardware registers**

| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| --- | --- | --- | --- | --- | --- | --- |
| VRM | Data retention mode(1) | STOP mode (or RESET) | 1.65 | - | - | V |

1. Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode).

**Flash memory and data EEPROM**

**Table 46. Flash memory and data EEPROM characteristics**

| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max(1)** | **Unit** |
| --- | --- | --- | --- | --- | --- | --- |
| VDD | Operating voltage  Read / Write / Erase | - | 1.65 | - | 3.6 | V |
| tprog | Programming time for word or half-page | Erasing | - | 3.28 | 3.94 | ms |
| Programming | - | 3.28 | 3.94 |

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**Table 46. Flash memory and data EEPROM characteristics**

| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max(1)** | **Unit** |
| --- | --- | --- | --- | --- | --- | --- |
| IDD | Average current during the whole programming / erase operation | TA = 25 °C, VDD = 3.6 V | - | 500 | 700 | µA |
| Maximum current (peak) during the whole  programming / erase operation | - | 1.5 | 2.5 | mA |

1. Guaranteed by design.

**Table 47. Flash memory and data EEPROM endurance and retention**

| **Symbol** | **Parameter** | **Conditions** | **Value** | **Unit** |
| --- | --- | --- | --- | --- |
| **Min(1)** |
| NCYC(2) | Cycling (erase / write)  Program memory | TA = –40°C to 105 °C | 10 | kcycles |
| Cycling (erase / write)  EEPROM data memory | 100 |
| Cycling (erase / write)  Program memory | TA = –40°C to 125 °C | 0.2 |
| Cycling (erase / write)  EEPROM data memory | 2 |
| tRET(2) | Data retention (program memory) after 10 kcycles at TA = 85 °C | TRET = +85 °C | 30 | years |
| Data retention (EEPROM data memory) after 100 kcycles at TA = 85 °C | 30 |
| Data retention (program memory) after 10 kcycles at TA = 105 °C | TRET = +105 °C | 10 |
| Data retention (EEPROM data memory) after 100 kcycles at TA = 105 °C |
| Data retention (program memory) after 200 cycles at TA = 125 °C | TRET = +125 °C |
| Data retention (EEPROM data memory) after 2 kcycles at TA = 125 °C |

1. Guaranteed by characterization results.

2. Characterization is done according to JEDEC JESD22-A117.

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**STM32L031x4/6 Electrical characteristics**

**6.3.10 EMC characteristics**

Susceptibility tests are performed on a sample basis during device characterization. **Functional EMS (electromagnetic susceptibility)**

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

• **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.

• **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to VDD and VSS through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 48*. They are based on the EMS levels and classes defined in application note AN1709.

**Table 48. EMS characteristics**

| **Symbol** | **Parameter** | **Conditions** | **Level/ Class** |
| --- | --- | --- | --- |
| VFESD | Voltage limits to be applied on any I/O pin to induce a functional disturbance | VDD = 3.3 V, LQFP48, TA = +25 °C, fHCLK = 32 MHz  conforms to IEC 61000-4-2 | 3B |
| VEFTB | Fast transient voltage burst limits to be applied through 100 pF on VDD and VSS  pins to induce a functional disturbance | VDD = 3.3 V, LQFP48, TA = +25 °C, fHCLK = 32 MHz  conforms to IEC 61000-4-4 | 4A |

**Designing hardened software to avoid noise problems**

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. Please note that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as: • Corrupted program counter

• Unexpected reset

• Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

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To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

**Electromagnetic Interference (EMI)**

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 49. EMI characteristics**

| **Symbol** | **Parameter** | **Conditions** | **Monitored**  **frequency band** | **Max vs.**  **fOSC/fCPU** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| **8 MHz/32 MHz** |
| SEMI | Peak level | VDD = 3.6 V,  TA = 25 °C,  LQFP48 package  conforming to IEC61967-2 | 0.1 to 30 MHz | –10 | dBµV |
| 30 to 130 MHz | 5 |
| 130 MHz to 1GHz | –5 |
| EMI Level | 1.5 | - |

**6.3.11 Electrical sensitivity characteristics**

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

**Electrostatic discharge (ESD)**

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

**Table 50. ESD absolute maximum ratings**

| **Symbol** | **Ratings** | **Conditions** | **Class** | **Maximum**  **value(1)** | **Unit** |
| --- | --- | --- | --- | --- | --- |
| VESD(HBM) | Electrostatic discharge voltage (human body model) | TA = +25 °C,  conforming to  ANSI/JEDEC JS-001 | 2 | 2000 | V |
| VESD(CDM) | Electrostatic discharge voltage (charge device model) | TA = +25 °C,  conforming to  ANSI/ESD STM5.3.1. | C4 | 500 |

1. Guaranteed by characterization results.

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**STM32L031x4/6 Electrical characteristics**

**Static latch-up**

Two complementary static tests are required on six parts to assess the latch-up performance:

• A supply overvoltage is applied to each power supply pin • A current injection is applied to each input, output and configurable I/O pin These tests are compliant with EIA/JESD 78A IC latch-up standard.

**Table 51. Electrical sensitivities**

| **Symbol** | **Parameter** | **Conditions** | **Class** |
| --- | --- | --- | --- |
| LU | Static latch-up class | TA = +125 °C conforming to JESD78A | II level A |

**6.3.12 I/O current injection characteristics**

As a general rule, current injection to the I/O pins, due to external voltage below VSS or above VDD (for standard pins) must be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

**Functional susceptibility to I/O current injection**

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence oscillator frequency deviation).

The test results are given in the *Table 52*.

**Table 52. I/O current injection susceptibility**

| **Symbol** | **Description** | **Functional susceptibility** | | **Unit** |
| --- | --- | --- | --- | --- |
| **Negative**  **injection** | **Positive**  **injection** |
| IINJ | Injected current on BOOT0 | –0 | NA(1) | mA |
| Injected current on PA0, PA2, PA4, PA5, PC15, PH0 and PH1 | –5 | 0 |
| Injected current on any other FT and FTf pin | –5 (2) | NA(1) |
| Injected current on any other pin | –5 (2) | +5 |

1. Current injection is not possible.

2. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

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**Electrical characteristics STM32L031x4/6**

**6.3.13 I/O port characteristics**

**General input/output characteristics**

Unless otherwise specified, the parameters given in *Table 53* are derived from tests performed under the conditions summarized in *Table 20*. All I/Os are CMOS and TTL compliant.

**Table 53. I/O static characteristics**

| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| --- | --- | --- | --- | --- | --- | --- |
| VIL | Input low level voltage | TC, FT, FTf, RST I/Os | - | - | 0.3VDD | V |
| BOOT0 pin | - | - | 0.14VDD(1) |
| VIH | Input high level voltage | All I/Os | 0.7 VDD | - | - |
| Vhys | I/O Schmitt trigger voltage hysteresis (2) | Standard I/Os | - | 10% VDD(3) | - |
| BOOT0 pin | - | 0.01 | - |
| Ilkg | Input leakage current (4) | VSS ≤VIN ≤VDD  All I/Os except  PA11, PA12, BOOT0 and FTf I/Os | - | - | ±50 | nA |
| VSS ≤VIN ≤VDD  PA11 and P12 I/Os | - | - | –50/+250 |
| VSS ≤VIN ≤VDD  FTf I/Os | - | - | ±100 |
| VDD≤VIN ≤5 V  All I/Os except for PA11, PA12, BOOT0 and FTf I/Os | - | - | 200 |
| VDD≤VIN ≤5 V  FTf I/Os | - | - | 500 |
| VDD≤VIN ≤5 V  PA11, PA12 and BOOT0 | - | - | 10 | µA |
| RPU | Weak pull-up equivalent resistor(5) | VIN = VSS | 25 | 45 | 65 | kΩ |
| RPD | Weak pull-down equivalent resistor(5) | VIN = VDD | 25 | 45 | 65 | kΩ |
| CIO | I/O pin capacitance | - | - | 5 | - | pF |

1. Guaranteed by characterization.

2. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results. 3. With a minimum of 200 mV. Guaranteed by characterization results.

4. The max. value may be exceeded if negative current is injected on adjacent pins.

5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

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